INCH-POUND
MIL-PRF-28750D
1 February 1999
SUPERSEDING
MIL-R-28750C
16 February 1993

PERFORMANCE SPECIFICATION

RELAYS, SOLID-STATE, GENERAL SPECIFICATION FOR

This specification is approved for use by all Departments and Agencies of the Department of Defense.

1. SCOPE

1.1 Scope. This specification covers the general requirements for hermetically sealed or encapsulated solid-state relays (SSR's) (see 6.1), incorporating semiconductor, microelectronic, and passive circuit devices.

1.2 SSR classification.

a. Class I (discrete) technology: SSR utilizing this type of technology, employs only discrete type components, which can be nonhermetically sealed. The completed SSR is hermetically sealed.

b. Class II (hybrid) technology: SSR utilizing this type of technology, employs chip (die) and wire bond technology. The completed SSR is hermetically sealed.

1.3 Part or Identifying Number (PIN). The PIN will consist of the designator, the basic number of the specification sheet, an assigned dash number (see 3.1), and a screening level that indicates the level of quality and reliability (see 1.3.1).

M	28750/5	-001	Y
Designator	Specification sheet	Dash number	Screening level (see 1.3.1)

1.3.1 Screening level. The screening level is identified by a single letter, Y or W. Use screening level Y for high reliability applications (see 3.7); and screening level W for general purpose applications (see 4.4, 4.5e, and 4.6.1.2b).

Beneficial comments (recommendations, additions, deletions) and any pertinent data which may be of use in improving this document should be addressed to Defense Supply Center, Columbus, Post Office Box 3990, Columbus, OH 43216-5000, by using the Standardization Document Improvement Proposal (DD Form 1426) appearing at the end of this document or by letter.

AMSC N/A FSC 5945

2. APPLICABLE DOCUMENTS

2.1 General. The documents listed in this section are specified in sections 3 and 4 of this specification. This section does not include documents cited in other sections of this specification or recommended for additional information or as examples. While every effort has been made to ensure the completeness of this list, document users are cautioned that they must meet all specified requirements documents cited in sections 3 and 4 of this specification, whether or not they are listed.

2.2 Government documents.

2.2.1 Specifications, standards, and handbooks. The following specifications, standards, and handbooks form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those listed in the issue of the Department of Defense Index of Specifications and Standards (DoDISS) and supplement thereto, cited in the solicitation (see 6.2).

SPECIFICATIONS

DEPARTMENT OF DEFENSE

MIL-C-17	-	Cables, Radio Frequency, Flexible And Semirigid, General Specification for.
MIL-PRF-19500	-	Semiconductor Devices, General Specification for.
MIL-PRF-38534	-	Hybrid Microcircuits, General Specification for

(See supplement 1 for list of specification sheets.)

STANDARDS

FEDERAL

FED-STD-H28	-	Screw-Thread Standards for Federal Services.

DEPARTMENT OF DEFENSE

MIL-STD-202	-	Test Methods for Electronic and Electrical Component Parts.
MIL-STD-750	-	Test Methods for Semiconductor Devices.
MIL-STD-790	-	Standard Practice for Established Reliability and High Reliability Qualified Products List (QPL) Systems for Electrical, Electronic, and Fiber Optic Parts Specifications.
MIL-STD-883	-	Test Method Standard, Microcircuits.
MIL-STD-1285	-	Marking of Electrical and Electronic Parts.

(Unless otherwise indicated, copies of the above specifications, standards, and handbooks are available from the Defense Automated Printing Service, Building 4D (DPM-DODSSP), 700 Robbins Avenue, Philadelphia, PA 19111-5094.)

2.3 Non-Government publications. The following documents form a part of this document to the extent specified herein. Unless otherwise specified, the issues of the documents which are DoD adopted are those listed in the issue of the DoDISS cited in the solicitation. Unless otherwise specified, the issues of documents not listed in the DoDISS are the issues of the documents cited in the solicitation (see 6.2).

AMERICAN NATIONAL STANDARDS INSTITUTE (ANSI)

ANSI Y32.2	-	Graphic Symbols for Electrical and Electronics Diagrams (Including Reference Designation, Class Designation Letters).

(Application for copies should be addressed to the American National Standards Institute, 1420 Broadway, New York, New York 10018.)

ELECTRONIC INDUSTRIES ASSOCIATION (EIA)

EIA-557 - Statistical Process Control Systems.

(Application for copies should be addressed to the Electronic Industries Association, 2001 Eye Street, N.W., Washington, DC 20026.)

2.4 Order of precedence. In the event of a conflict between the text of this document and the references cited herein (except for associated detail specifications, specification sheets or MS standards), the text of this document will take precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Specification sheets. The individual item requirements shall be as specified herein and in accordance with the applicable specification sheet. In the event of conflict between requirements of this specification and the specification sheet, the latter shall govern.

3.2 Qualification. SSR's furnished under this specification shall be products which are authorized by the qualifying activity for listing on the applicable Qualified Products List (QPL) at the time of award of contract (see 4.4 and 6.3).

3.3 QPL system. The manufacturer shall establish and maintain a QPL system for parts covered by this specification. Requirements for this system are specified in MIL-STD-790. For class II SSR's, the manufacturer’s QPL system shall also address the requirements of appendix A and the qualifying activity for this specification may use pre-existing certification of the manufacturing facility in accordance with MIL-PRF-38534 as an alternative. The manufacture shall also establish a component evaluations system as part of the MIL-STD-790 overall system in accordance with appendix B.

3.3.1 Statistical process control (SPC). As part of the overall MIL-STD-790 QPL system, the manufacturer shall establish an SPC system that meets the requirements of EIA-557.

3.3.2 Electrostatic discharge (ESD) control program. As part of the overall MIL-STD-790 QPL system, the manufacturer shall establish and maintain an ESD control system. As a minimum, this program shall address the identification of ESD sensitive (ESDS) sub-components and end items, facilities, training design protection, handling procedures, marking, cleaning, packaging, and verification.

3.4 Materials. Materials shall be as specified herein. However, when a definite material is not specified, a material shall be used which will enable the SSR's to meet the performance requirements of this specification. Materials used shall be self-extinguishing; and shall not support combustion, give off noxious gases in harmful quantities, give off gases in quantities sufficient to cause explosion of sealed enclosures, cause contamination to any part of the SSR, or form current carrying tracks when subjected to any of the tests specified herein. The selection of materials shall be such as to provide maximum shelf life. After qualification, any change of parts or material shall be submitted to the Government qualifying activity for approval. Acceptance or approval of any constituent material shall not be construed as a guaranty of the acceptance of the finished product.

3.5 Circuit element requirements for class II SSR's. The requirements for circuit elements shall be in accordance with appendix B.

3.6 Interface and physical dimensions. SSR's shall meet the interface and physical dimensions specified (see 3.1).

3.6.1 Threaded parts. All threaded parts shall be in accordance with FED-STD-H28. Where practical, all threads shall be in conformity with the coarse-thread series. The fine-thread series may be used only for applications that show a definite advantage through their use. Where a special diameter-pitch combination is required, the thread shall be of American National Form and of any pitch between 16 and 36, which is used in the fine-thread series. Terminal threads shall be class 2A and class 2B for external and internal threads, respectively.

3.6.2 Envelope (case, cover, or enclosure). SSR's with metal cases shall be provided with means to permit assured contact to ground. The enclosure shall not be electrically connected to any terminal, except one provided specifically for grounding or as specified (see 3.1).

3.6.3 Sealing process. Sealed SSR's shall be dried, degassed, and backfilled (see 6.7) with an atmosphere and sealed by welding such that the requirements of this specification are met (see 3.9). Adjunct sealant, if used, shall comply with the following:

a. Sealant shall not extend beyond 20 percent of the length of the exposed terminals above the glass meniscus.

b. Trace color is permitted if it is a natural result of the sealant process.

c. After curing, sealant shall form a permanent nonconductive, noncracking seal under all relay environments.

3.6.4 Mounting means. Mounting means shall be as specified (see 3.1).

3.6.4.1 Socket. Plug-in SSR's shall be so designed that the weight of the SSR will be supported, and the stability of the mounting will be provided by means other than the terminals.

3.6.5 Terminals (see 3.1). Terminals shall be as specified herein.

3.6.5.1 Solder-lug terminals. Solder-lug terminals shall be designed to accommodate two conductors, each rated to carry the maximum rated current of the contact or coil terminated.

3.6.5.2 Wire leads. Wire leads shall be as specified (see 3.1).

3.6.5.3 Plug-in termination. Plug-in terminations shall conform to the arrangements or dimensions and interfaces necessary for proper mating with the associated connectors or sockets as specified (see 3.1). The mounting arrangement of the SSR and its corresponding socket shall be so designed that the entire weight of the SSR will be suspended and the stability of its mounting will be provided by an auxiliary mounting means other than the electrical terminals of the socket (see 3.1). During qualification, SSR's with plug-in terminals shall have electrical tests of section 4 and environmental tests of section 4 performed with the appropriate or specified socket or connector assembled to the SSR. For further guidance on lead finishes see 6.6.2.

3.6.5.4 Screw. Screw terminals shall be supplied with one nut, capable of engaging the screw by at least three full threads, two flat washers and one lock washer. The size of screw thread and length shall be as specified (see 3.1). At least three full threads of the screw shall visibly protrude with all hardware tightened in place.

3.6.6 Circuit diagram. The circuit diagram as specified (see 3.1), shall be a terminal view. Circuit symbols shall be in accordance with ANSI Y32.2. For SSR's without an orientation tab, the circuit diagram as specified (see 3.1), shall be orientated so that when the SSR is held with the circuit diagram right-side up as shown in the appropriate specification sheet (see 3.1), and rotated away from the viewer about a horizontal axis through the diagram until the header terminals face the viewer, then each terminal shall be in the location shown on the circuit diagram.

3.6.7 Temperature. Unless otherwise specified (see 3.1), the SSR shall operate satisfactorily throughout the temperature range of -55°C to +125°C, and shall not be damaged when stored at a temperature in the range of -55°C to +125°C.

3.6.8 Package. The outline dimensions of the package shall be as specified (see 3.1). In addition, the relay shall meet the following requirements:

3.6.8.1 Class I. Discrete technology SSR's supplied under this specification shall be sealed in glass, metal, or ceramic (or combination of these) packages. Adhesive or polymeric material shall not be used for package cover/lid attachment, seal, or repair. Use of any other package material shall require prior approval from the qualifying authority.

3.6.8.2 Class II. Hybrid technology SSR's supplied to this specification shall be hermetically sealed in glass, metal, or ceramic (or combinations of these) packages. No adhesive or polymeric materials shall be used for package lid attach (or seal) or repair. Flux shall not be used in the final sealing process. The minimum distance between the glass to metal seals and the package sealing surface for seam welded packages after final seal shall be 0.040 inch (1.02 mm) minimum.

3.6.8.3 Internal water vapor content. The internal water vapor content shall not exceed 5,000 parts per million at +100°C. Polymer impregnation or secondary seal (backfill, coating, or other uses of organic or polymeric materials to effect, improve, or repair the seal) of the SSR package shall not be permitted.

NOTE: Packages containing beryllia shall not be ground, sandblasted, machined, or have other operations performed on them which will produce beryllia or beryllium dust. Furthermore, beryllium oxide packages shall not be placed in acids that will produce fumes containing beryllium.

3.6.9 Metals. Metal surfaces shall be corrosion resistant or shall be plated or treated to resist corrosion and shall meet the requirements specified in 3.6.11.

3.6.10 Other materials. External parts, elements or coatings including markings shall be non-nutrient to fungus and shall not blister, crack, outgas, soften, flow, or exhibit defects that adversely affect storage, operation, or environmental capabilities of SSR's delivered to this specification under the specified test conditions.

3.6.11 Package and lead materials and finishes.

3.6.11.1 Lead or terminal material. A lead or terminal material that enables the relay to meet all of the performance requirements of this specification shall be used. For further guidance on lead and terminal materials that meet the performance requirements of this specification, see 6.6.1.

3.6.11.2 Lead finish. The finish system on all external leads or terminals shall conform to one of the following:

a. Hot solder dip.

b. Tin-lead plate.

c. Gold plate.

Pure tin finish shall not be used on any internal or external package surface or as a lead finish unless tin whisker growth has been inhibited. (NOTE: For further guidance on lead finishes, see 6.6.2)

3.6.11.3 Solder dip (retinning) leads. Only the manufacturer, at their option, may solder dip/retin the leads of the product supplied to this specification provided the solder dip/retin process (see appendix A, paragraph A3.6.3) has been approved by the qualifying activity.

3.6.11.4 Package body finish. External metallic package elements other than leads or terminals (e.g., lids, covers, bases, seal rings, etc.) shall meet the applicable corrosion resistance and environmental requirements or shall be finished so that they meet those requirements using finishes conforming to one or more of the following as applicable (pure tin finish shall not be used on any internal or external package surface or as a lead finish. In addition, tin plating shall not be used as an undercoat):

a. Solder.

b. Tin-lead plate.

c. Gold plate.

d. Nickel plate.

(NOTE: For further guidance on these package body finishes, see 6.6.3).

3.7 Screening. When SSR's (screening level Y only) are screened as specified in 4.7.2, they shall meet the requirements as specified in 3.7.1 through 3.7.7.

3.7.1 Preseal burn-in (optional). When SSR's are tested as specified in 4.7.2.1, they shall show no evidence of physical or mechanical damage. In addition, SSR's shall be tested in accordance with the electrical characteristics (see 3.12) at 25°C. Manufacturer may also perform electrical tests at temperature extremes.

3.7.2 Internal visual. When SSR's are tested as specified in 4.7.2.2, they shall meet the requirements as specified.

3.7.3 Temperature cycling. When SSR's are tested as specified in 4.7.2.3, they shall show no evidence of physical or mechanical damage.

3.7.4 Mechanical shock or constant acceleration. When SSR's are tested as specified in 4.7.2.4, they shall show no signs of physical or mechanical damage.

3.7.5 Load conditioning. When SSR's are tested as specified in 4.7.2.5, they shall show no signs of physical or mechanical damage.

3.7.6 Interim (pre-burn-in) electrical requirements (optional). When SSR's are tested as specified in 4.7.2.6, they shall meet the electrical requirements as applicable.

3.7.7 Burn-in test. When SSR's are tested as specified in 4.7.2.7, they shall show no signs of physical or mechanical damage.

3.8 Solderability (applicable to solder terminals). When SSR's are tested as specified in 4.7.3, the dipped surface of solid wire-lead and pin terminals shall be at least 95 percent covered with a continuous new solder coating. The remaining 5 percent may contain only small pinholes or rough spots; these shall not be concentrated in one area. Bare base metal where the solder dip failed to cover the original coating is an indication of poor solderability, and shall be cause for failure. For solder-lug terminals, 95 percent of the total length of fillet, which is between the standard wrap wire and the terminal, shall be tangent to the surface of the terminal being tested, and shall be free of pinholes, voids, etc. A ragged or interrupted line at the point of tangency between the fillet and the terminal under test shall be a failure.

3.9 Seal. When tested as specified in 4.7.4, there shall be no leakage in excess of 1×10^{-8} atmospheric cubic centimeters per second of air (atm cm^3/s), or as specified (see 3.1).

3.10 Insulation resistance. When SSR's are tested as specified in 4.7.5, the resistance shall be 100 megohms minimum. When specified (see 3.1), the insulation resistance between load circuits and input shall be 50 megohms minimum.

3.11 Dielectric withstanding voltage (DWV). When tested as specified in 4.7.6, SSR's shall withstand the voltage specified without damage; shall not have leakage current in excess of 1.2 milliampere (mA); and there shall be no evidence of damage due to arcing (air discharge), flashover (surface discharge), or insulation breakdown (puncture discharge).

3.12 Electrical characteristics. Unless otherwise specified, 100 percent of the electrical characteristics shall be tested at -55°C, +25°C, and +125°C. Manufacturer has the option for sequence of test temperature (+25°C, -55°C, +125°C), and the sequence in which the electrical characteristics tests are performed.

3.12.1 Reverse polarity (dc operated SSR's) (when specified, see 3.1). When tested as specified in 4.7.7.1, the SSR shall not operate or be damaged. Following the test, the turn-on voltage, input current, and turn-off voltage shall be as specified (see 3.1).

3.12.2 Input current (when specified, see 3.1). When SSR's are tested as specified in 4.7.7.2.1, the input current shall be as specified (see 3.1).

3.12.3 Input turn-on voltage (when specified, see 3.1). When SSR's are tested as specified in 4.7.7.2.2, the SSR shall operate as specified (see 3.1).

3.12.4 Input turn-off voltage (when specified, see 3.1). When SSR's are tested as specified in 4.7.7.2.3, the SSR shall operate as specified (see 3.1).

3.12.5 Bias current (when specified, see 3.1). When SSR's are tested as specified in 4.7.7.2.4, the bias current shall not exceed the specified value (see 3.1).

3.12.6 Control current (when specified, see 3.1). When SSR's are tested as specified in 4.7.7.2.5, the control current shall not exceed the specified value (see 3.1).

3.12.7 Control turn-on voltage (when specified, see 3.1). When SSR's are tested as specified in 4.7.7.2.6, the SSR shall operate as specified (see 3.1).

3.12.8 Control turn-off voltage (when specified, see 3.1). When SSR's are tested as specified in 4.7.7.2.7, the SSR shall operate as specified (see 3.1).

3.12.9 Overload - Will-not-trip current (short circuit protected SSR's) (when specified, see 3.1). When SSR's are tested as specified in 4.7.7.3, the SSR shall remain ON for the specified time (see 3.1).

3.12.10 Overload - Must-trip current (short circuit protected SSR's) (when specified, see 3.1). When SSR's are tested as specified in 4.7.7.4, the SSR shall shut OFF within the specified time (see 3.1).

3.12.11 Turn-on into a shorted load (when specified, see 3.1). When SSR's are tested as specified in 4.7.7.5, the SSR shall shut OFF.

3.12.12 Shorted load with SSR ON (when specified, see 3.1). When SSR's are tested as specified in 4.7.7.6, the SSR shall shut OFF.

3.12.13 Status turn-on time (when specified, see 3.1). When SSR's are tested as specified in 4.7.7.7, the status turn-on time shall not exceed the specified value (see 3.1).

3.12.14 Status "ON" voltage (when specified, see 3.1). When SSR's are tested as specified in 4.7.7.8, the status "ON" voltage shall be as specified (see 3.1).

3.12.15 Status turn-off time (when specified, see 3.1). When SSR's are tested as specified in 4.7.7.9, the status turn-off time shall not exceed the specified value.

3.12.16 Status "OFF" voltage (when specified, see 3.1). When SSR's are tested as specified in 4.7.7.10, the status "OFF" voltage shall be as specified (see 3.1).

3.12.17 Status blocking voltage (when specified, see 3.1). When SSR's are tested as specified in 4.7.7.11, the status (off) current shall not exceed the specified value.

3.12.18 Status leakage current (when specified, see 3.1). When SSR's are tested as specified in 4.7.7.12, the status leakage current shall not exceed the specified value.

3.12.19 Turn-on time. When SSR's are tested as specified in 4.7.7.13, the turn-on time shall not exceed the specified value (see 3.1).

3.12.20 Turn-off time. When SSR's are tested as specified in 4.7.7.14, the turn-off time shall not exceed the specified value (see 3.1).

3.12.21 Output voltage drop. When SSR's are tested as specified in 4.7.7.15, the output voltage drop shall not exceed the value specified (see 3.1).

3.12.22 Output leakage current. When SSR's are tested as specified in 4.7.7.16, the leakage current in the output circuit shall not exceed the specified value (see 3.1).

3.12.23 Transient Voltage (when specified, see 3.1). When SSR's are tested as specified in 4.7.7.17, the output shall not turn on. (see 3.1).

3.12.24 DC offset voltage (ac SSR's only) (when specified, see 3.1). When SSR's are tested as specified in 4.7.7.18, the dc offset voltage shall not exceed the specified value (see 3.1).

3.12.25 Waveform distortion (ac SSR's only) (when specified, see 3.1). When SSR's are tested as specified in 4.7.7.19, the waveform distortion (commutation spikes) shall not exceed the specified value (see 3.1).

3.12.26 Minimum load current rating (ac SSR's only) (when specified, see 3.1). When SSR's are tested as specified in 4.7.7.20, the SSR shall remain ON.

3.12.27 Exponential rate of voltage rise (when specified, see 3.1). When SSR's are tested as specified in 4.7.7.21, they shall withstand the specified rate of voltage rise (see 3.1).

3.12.28 Zero crossover (ac SSR's only) (when specified, see 3.1). When SSR's are tested as specified in 4.7.7.22, the SSR turn-on shall occur within the specified (see 3.1) zero voltage crossover, and SSR turn-off shall occur within the specified (see 3.1) zero current crossover.

3.12.29 Electrical system spike (when specified, see 3.1). When SSR's are tested as specified in 4.7.7.23, they shall withstand the voltage specified without damage.

3.12.30 Overload (non-short circuit protected SSR's only) (when specified, see 3.1). When SSR's are tested as specified in 4.7.7.24, they shall withstand the specified overload without damage.

3.12.31 Power dissipation (when specified, see 3.1). When SSR's are tested as specified in 4.7.7.25, the power dissipation shall not exceed the specified value (see 3.1).

3.13 Resistance to solvents. When SSR's are tested as specified in 4.7.8, the marking shall remain legible.

3.14 Shock (specified pulse). When SSR's are tested as specified in 4.7.9, there shall be no evidence of physical or mechanical damage.

3.15 Vibration. When SSR's are tested as specified in 4.7.10, there shall be no evidence of physical or mechanical damage.

3.16 Terminal strength. When SSR's are tested as specified in 4.7.11, there shall be no evidence of loosening or breaking of the terminals; there shall be no deformation to the threads of screw terminals; no damage to the insulating base of plug-in SSR's; nor shall there be any other damage which would adversely affect the normal operation of the SSR. Bending of solder terminals shall not be construed as damage; bending of plug-in terminals shall not be construed as damage, provided they can be reformed in a manner to permit proper mating with the applicable sockets.

3.17 Moisture resistance (applicable to nonhermetically sealed SSR's only). When SSR's are tested as specified in 4.7.12, there shall be no evidence of breaking, cracking, chipping or flaking of the finish, or loosening of the terminals. After the 24-hour drying period, SSR's shall meet the following requirements:

a. Insulation resistance: as specified in 3.10.

b. DWV: as specified in 3.11.

c. Input Turn-off voltage: as specified in 3.12.4.

d. Input Turn-on voltage: as specified in 3.12.3.

e. Output voltage drop: as specified in 3.12.21.

f. Output leakage current: as specified in 3.12.22.

3.18 Crosstalk (when specified, see 3.1). When SSR's are tested as specified in 4.7.13, the attenuation shall be a minimum of 20 decibels.

3.19 Isolation (when specified, see 3.1). When SSR's are tested as specified in 4.7.14, the capacitance shall not exceed the value specified.

3.20 Resistance to soldering heat (when specified, see 3.1). When SSR's are tested as specified in 4.7.15, there shall be no damage which could adversely affect normal operation of the SSR's.

3.21 Salt atmosphere (corrosion). When SSR's are tested as specified in 4.7.16, there shall be no evidence of breaking, cracking, chipping or flaking of the finish, nor exposure of base metal due to corrosion which could adversely affect the application or performance characteristics of the SSR's.

3.22 Life. When SSR's are tested as specified in 4.7.17, there shall be no damage which could adversely affect normal operation of the SSR's.

3.23 Marking. All applicable marking shall appear on a surface visible when the SSR is mounted in its normal position.

3.23.1 JAN and J marking. The United States Government has adopted, and is exercising legitimate control over the certification marks "JAN" and "J", respectively, to indicate that items so marked or identified are manufactured to, and meet all the requirements of specifications. Accordingly, items acquired to and meeting all of the criteria specified herein and in applicable specifications, shall bear the certification mark "JAN" except that items too small to bear the certification mark "JAN" shall bear the letter "J". The "JAN" or "J" shall be placed immediately before the part number except that if such location would place a hardship on the manufacturer in connection with such marking, the “JAN” or “J” may be located on the first line above or below the part number. Items furnished under contracts or orders which either permit or require deviation from the conditions or requirements specified herein or in applicable specifications shall not bear "JAN" or "J". In the event an item fails to meet the requirements of this specification and the applicable specification sheets or associated specifications, the manufacturer shall remove completely the part number the "JAN" or the "J" from the sample tested and also from all items represented by the sample. The "JAN" or "J" certification mark shall not be used on products acquired to contractor drawings or specifications. The United States Government has obtained

Certificate of Registration No. 504,860 for the certification mark "JAN" and Registration Number 1,586,261 for the certification mark “J”.

3.23.2 Identification marking (full). SSR's shall be marked in accordance with MIL-STD-1285, with the following information as a minimum:

a. Military PIN, including a ”Y” or “W” to indicate screening level (see 1.3 and 3.1). The “JAN” or “J” shall not be marked in front of the PIN.

b. "JAN" or "J" brand. The "JAN" or "J" shall appear directly above or below the "M" of the PIN.

examples: JAN or M28750/5-001Y
M28750/5-001Y J

c. Rated input voltage.

d. Rated output voltage (or current).

e. Circuit diagram.

f. Terminal marking (see 3.6.5).

g. Date code (at the option of the manufacturer the "J" with the date code may be used instead of b).

h. Manufacturer's name or Commercial and Government Entity (CAGE) code.

i. Lot symbol.

j. ESD sensitivity identifier, (see 3.23.4).

3.23.3 Minimum marking (when specified, see 3.1). When space does not permit the marking specified in 3.23.2, the marking shall include, as a minimum, the part number including a “Y” to indicate screening level, “J” with date code (example “J9232”), circuit diagram, manufacturer's name or CAGE code, and ESD identifier. The circuit diagram may also be eliminated provided that it appears in the SSR specification.

3.23.4 ESD sensitivity identifier. The SSR shall be marked with a sensitive electronic device symbol as specified in MIL-STD-1285, or if room does not permit, the outline of an equilateral triangle (i.e. Δ) shall be used and may also be used as a pin 1 identifier. The equilateral triangle will designate these SSR's as ESDS in the range of 0 volts - 1,999 volts and the parts shall be handled as such same as previous revision.

3.23.5. Beryllium oxide package identifier. If a SSR package contains beryllium oxide, the SSR shall be marked with the designation “BeO”.

3.24 Recycled, recovered, or environmentally preferable materials. Recycled, recovered, or environmentally preferable materials should be used to the maximum extent possible provided that the material meets or exceeds the operational and maintenance requirements, and promotes economically advantageous life cycle costs.

3.25 Workmanship. SSR's shall be manufactured and processed in such a manner as to be uniform in quality and shall be free from any defects that will affect life, serviceability or appearance.

4. VERIFICATION

4.1 Classification of inspections. The inspections specified herein are classified as follows:

a. Qualification inspection (see 4.4).

b. Conformance inspection (see 4.6).

c. Periodic inspection (group B and group C inspection, see 4.6.2).

4.2 QPL system. The manufacturer shall establish and maintain a QPL system as described in 3.3. Evidence of such compliance shall be verified by the qualifying activity for this specification as prerequisite for qualification and retention of qualification.

4.3 Inspection conditions. Unless otherwise specified herein, all inspections shall be performed in accordance with the test conditions specified in the "GENERAL REQUIREMENTS" of MIL-STD-883 and MIL-STD-202.

4.3.1 Power supply. Unless otherwise specified herein, the power supply shall have no more than 5 percent regulation at 110 percent of the specified test current. A dc power supply shall have no more than 5 percent ripple voltage. An ac power supply shall be within 1 percent of the specified frequency and shall be sinusoidal with a form factor between 0.95 and 1.25.

4.3.1.1 Grounding. Unless otherwise specified (see 3.1), the negative side of the dc power supply shall be grounded; one side of single-phase ac power supply shall be grounded; or the neutral of three-phase ac power supply shall be grounded, as applicable.

4.3.2 Load conditions during tests. The input of the SSR being tested shall be connected to the grounded side of its power supply; each load of the SSR being tested shall be connected to the grounded side of its power supply; and each output shall be connected to an individual load. Separate power supplies shall be used for the input to the SSR and the individual load being tested.

4.4 Qualification inspection. Qualification inspection shall be performed at a laboratory acceptable to the Government (see 6.3) on sample SSR's produced with equipment and procedures normally used in production.

Qualification of the “W” screening level part number is predicated upon qualification of the “Y” screening level part number. Upon request of the manufacturer, qualification to the “W” screening level part numbers will be granted for the envelope of products successfully qualified to the “Y” screening level part numbers. The products involved shall be of the same design, manufactured using the same facilities, processes, and materials as the product originally submitted for and qualified under the “Y” screening level.

4.4.1 Sample size. The number of SSR's to be subjected to qualification inspection shall be 12. In addition, submit one unsealed sample to the qualifying activity as part of the qualification procedure. The sample SSR's shall be taken at random from a production run and shall be produced with equipment and procedures normally used in production, and which have been subjected to and passed the requirements of group A inspection (see 4.6.1.2). Qualification shall not be granted if group A inspection requirements are not complied with.

4.4.2 Inspection routine. Qualification samples shall be subjected to the tests as specified in table I, in the order shown, as applicable for each SSR. All sample units shall be subjected to group Q1. The sample units shall then be divided into three groups of four and shall then be subjected to group Q2, group Q3, and group Q4.

4.4.3 Failures. No failures shall be allowed for group Q1, and only one failure shall be allowed for group Q2, group Q3, and group Q4 combined. Failures in excess of those allowed shall be cause for refusal to grant qualification approval.

TABLE I. Qualification inspection.

Inspection	Requirement paragraph	Test Method paragraph	Sample per group
Group Q1			
Electrical system spike	3.12.29	4.7.7.23	12
Overload	3.12.30	4.7.7.24	
Power dissipation	3.12.31	4.7.7.25	
Visual and mechanical inspection	3.1, 3.4, 3.6, 3.23, and 3.24	4.7.1	
Group Q2			
Resistance to solvents	3.13	4.7.8	
Shock (specified pulse	3.14	4.7.9	
Vibration	3.15	4.7.10	
Terminal strength	3.16	4.7.11	4
Temperature cycling	3.7.3	4.7.2.3	
Seal	3.9	4.7.4	
Moisture resistance	3.17	4.7.12	
Insulation resistance	3.10	4.7.5	
DWV	3.11	4.7.6	
Electrical characteristics	3.12	4.7.7	
Visual and mechanical inspection	3.1, 3.4, 3.6, 3.23, and 3.24	4.7.1	
Group Q3			
Crosstalk	3.18	4.7.13	
Isolation	3.19	4.7.14	
Resistance to soldering	3.20	4.7.15	
heat	3.21	4.7.16	4
Salt atmosphere (corrosion)	3.10	4.7.5	
Insulation resistance	3.11	4.7.6	
DWV	3.12	4.7.7	
Electrical characteristics	3.9	4.7.4	
Seal	3.1, 3.4, 3.6, 3.23, and 3.24	4.7.1	
Visual and mechanical inspection			
Group Q4			
Life	3.22	4.7.17	
Insulation resistance	3.10	4.7.5	
DWV	3.11	4.7.6	4
Electrical characteristics	3.12	4.7.7	
Seal	3.9	4.7.4	
Visual and mechanical inspection	3.1, 3.4, 3.6, 3.23, and 3.24	4.7.1	

4.5 Retention of qualification. To retain qualification, every 24 months, the contractor shall provide verification of the following requirements:

a. MIL-STD-790 program.

b. Design of the SSR has not been modified.

c. Screening tests, conformance tests, and periodic tests have been performed as specified herein.

d. The contractor retains the capability to manufacture and test SSR's to this specification.

e. Continued qualification to screening level W shall be based on continued maintenance of qualification for screening level Y.

In the event that no production occurred during this period, the contractor shall still verify to the qualifying activity the capability to manufacture and test the QPL SSR still exists and the contractor wants to remain on the QPL.

4.6 Conformance inspection.

4.6.1 Inspection of product for delivery. Inspection shall consist of group A inspection.

4.6.1.1 Production and inspection lot.

4.6.1.1.1 Production lot. A production lot shall consist of all SSR's covered by a single specification sheet and single part number. All SSR's in the lot shall have been started, processed, assembled, and tested as a group. Lot identity shall be maintained throughout the manufacturing cycle.

4.6.1.1.2 Inspection lot. A inspection lot shall consist of all SSR's covered by a single specification sheet, produced and sealed under essentially the same conditions, and offered for inspection at one time within a period not to exceed 1 month.

4.6.1.2 Group A inspection.

a. Screening level Y: Group A inspection shall consist of the inspections specified in table II, in the order shown.

b. Screening level W: The manufacturer shall establish and maintain an inspection system to verify that these SSR's meet the electrical, visual, mechanical, and solderability requirements. In-line or process control may be part of such a system. The inspection system shall also include criteria for lot rejection and corrective actions. The inspection system shall be verified under the overall QPL system (see 3.3). NOTE: Since screening level W is the same design as screening level Y without the mandatory conformance inspection, screening level W product shall meet the environmental qualification type requirements (e.g., moisture resistance, shock, vibration, etc.).

4.6.1.2.1 Sampling plan (group A1, group A2, and group A3). The tests performed in group A1, group A2, and group A3 shall require 100 percent inspection, except only two units per production lot shall be tested for dc offset voltage, waveform distortion, and minimum current ratings. Defective SSR's shall be removed from the production lot. If, during the 100 percent inspection of A2 over 5 percent of the SSR's are discarded, the production lot shall be rejected. The rejected production lot may be resubmitted for A2 rescreening provided the SSR's meet the following criteria:

a. The observed percentage defective allowed (PDA) does not exceed twice the specified PDA.

b. The cause of failure has been evaluated and determined.

c. The failure was due to random causes; or, for pattern failures, appropriate and effective corrective action has been completed to reject all SSR's affected by the failure cause.

d. Appropriate preventive action has been initiated.

e. The failure shall not have the potential to cause any latent field failure on the remaining SSR's.

f. The preceding conditions shall not apply in those cases (instances) where the failures can be directly attributed to random equipment failure and/or operator error, with qualifying activity concurrence.

4.6.1.2.2 Sampling plan (A4). Two samples shall be selected randomly from each inspection lot and subjected to the A4 solderability test. The manufacturer may use electrical rejects from the A2 screening tests for all or part of the samples to be used for solderability testing. If there is one or more defects, the lot shall have failed.

4.6.1.2.2.1 Rejected lots (A4). In the event of one or more defects, the inspection lot is rejected. The manufacturer may use one of the following options to rework the lot:

a. Each production lot that was used to form the failed inspection lot shall be individually submitted to the solderability test as required in 4.6.1.2.2. Production lots that pass the solderability test are available for shipment. Production lots failing the solderability test can be reworked only if submitted to the solder dip procedure in (b).

b. The manufacturer submits the failed lot to a 100 percent solder dip using an approved solder dip process in accordance with 3.6.11.3. Following the solder dip process, the A2, A3, and A4 group A inspections shall be repeated on the lot. If the lot fails the A2 PDA requirement or fails the A4 solderability test, the lot shall be rejected and shall not be furnished against the requirements of this specification.

4.6.1.2.3 Disposition of samples. The solderability test is a destructive test and samples submitted to the solderability test shall not be supplied on the contract.

4.6.2 Periodic inspections. Periodic inspections shall consist of group B and group C. Except where the results of these inspections show noncompliance with the applicable requirements (see 4.6.2.2.4), delivery of products which have passed group A shall not be delayed pending the results of these periodic inspections.

4.6.2.1 Group B inspection. Group B inspection shall consist of the tests specified in table III and shall be made on sample units which have been subjected to and have passed the group A inspection.

4.6.2.1.1 Sampling plan. Four sample units from each specification sheet shall be selected every six months from sample SSR's which have passed group A inspection. No failures shall be allowed. If the manufacture can demonstrate this test has been performed for five consecutive times with zero failures, the frequency of this test, with the approval of the qualifying activity, can be performed on an annual basis. If the design, material, technology or processing of the part is changed, or if there are any quality problems or failures, the qualifying activity may require resumption of the original test frequency.

4.6.2.1.2 Disposition of sample units. Sample units which have been subjected to group B inspection shall not be delivered on the contract or purchase order.

4.6.2.2 Group C inspection. Group C inspection shall consist of the tests specified in table I, in the order shown. Group C inspection shall be made on sample units selected from inspection lots which have passed the group A inspection.

4.6.2.2.1 Sampling plan. Twelve sample SSR's of the same part number as originally qualified shall be selected 24 months after the date of every notification of qualification, and after each subsequent 24-month period.

4.6.2.2.2 Failures. Failures in excess of those allowed in table I shall be cause for removal of qualification.

4.6.2.2.3 Disposition of sample units. Sample units which have been subjected to group C inspection shall not be delivered on the contract or purchase order.

TABLE II. Group A inspection.

Inspection	Requirement paragraph	Test method paragraph	Sampling procedure
Group A1			
Screening	3.7	4.7.2	4.6.1.2.1
Group A2 1/ 2/			
Insulation resistance	3.10	4.7.5	
DWV	3.11	4.7.6	4.6.1.2.1
Electrical characteristics	3.12	4.7.7	
Group A3 4/ 5/			
Seal	3.9	4.7.4	4.6.1.2.1
Visual and mechanical inspection	3.1, 3.4, 3.6, 3.23, and 3.24	4.7.1	
Group A4			
Solderability 6/	3.8	4.7.3	4.6.1.2.2

1/ Testing sequence optional for insulation resistance and DWV.
2/ Transient voltage and exponential rate of voltage rise (dv/dt) shall be performed at +25°C ambient.
3/ Electrical characteristic testing shall not include the following: Electrical system spike, overload, and power dissipation.
4/ Physical dimensions and weight shall be measured on two sample units per lot.
5/ Minor defects, such as marking, may be reworked.
6/ This solderability test can be eliminated if the manufacturer has demonstrated process control under the SPC program (see 3.3.1), or other method that has been approved by the qualifying activity. If the design, material, technology, or processing of the part is changed or, if there are any quality problems, or failures, the qualifying activity may require resumption of the specified testing. Deletion of testing does not relieve the manufacturer from meeting the test requirement in case of dispute.

TABLE III. Group B inspection.

Inspection	Requirement paragraph	Test method paragraph	Number of sample units	Number of failure allowed
Vibration	3.15	4.7.10		
Terminal strength	3.16	4.7.11		
Moisture resistance	3.17	4.7.12		
Insulation resistance	3.10	4.7.5	4	0
Electrical characteristics	3.12	4.7.7		
Seal	3.9	4.7.4		
Visual and mechanical inspection	3.1, 3.4, 3.6, 3.23, and 3.24	4.7.1		

4.6.2.2.4 Noncompliance. If a sample fails the group B or group C inspection, the manufacturer shall notify the qualifying activity and the cognizant inspection activity of such failure and take corrective action on the materials or processes, or both, as warranted. This corrective action shall be performed on all units of product which can be corrected; which were manufactured under essentially the same materials and processes; and which are subject to the same failure. Acceptance and shipment of the product shall be discontinued until corrective action, acceptable to the qualifying activity, has been taken. After the corrective action has been taken, group C inspection shall be repeated on additional sample units (all inspections, or the inspection which the original sample failed, at the option of the qualifying activity). Group A and group B inspections may be reinstituted; however, final acceptance and shipment shall be withheld until the group C inspection has shown that the corrective action was successful. In the event of failure after reinspection, information concerning the failure shall be furnished to the cognizant inspection activity and the qualifying activity.

4.7 Methods of inspection.

4.7.1 Visual and mechanical inspection. SSR's shall be examined to verify that the interface, external design and technology, physical dimensions, marking, and workmanship are in accordance with the applicable requirements (see 3.1, 3.4, 3.6, 3.23 and 3.24).

4.7.2 Screening (Y level only) (see 3.7). SSR's shall be screened in accordance with 4.7.2.1 through 4.7.2.7.

4.7.2.1 Preseal burn-in (optional) (see 3.7.1). SSR's shall be tested in accordance with method 1030 of MIL-STD-883.

4.7.2.2 Internal visual (see 3.7.2). SSR's shall be tested in accordance with method 2017 of MIL-STD-883.

4.7.2.3 Temperature cycling (see 3.7.3). SSR's shall be tested in accordance with method 1010 of MIL-STD-883. Unless otherwise specified, test condition B shall apply; 100 cycles for qualification inspection and 10 cycles for quality conformance inspection.

4.7.2.4 Mechanical shock or constant acceleration (see 3.7.4).

a. Mechanical shock - SSR's shall be tested in accordance with MIL-STD-883, method 2002, test condition B. Y1 direction only.

b. Constant acceleration - SSR's shall be tested in accordance with MIL-STD-883, method 2001, test condition A. Y1 direction only.

4.7.2.5 Load conditioning (see 3.7.5). SSR's shall be cycled by applying a step function voltage to the input; the input shall be energized at zero or rated input voltage. The on-state load shall be maximum rated current, without auxiliary heat sink. Each output circuit shall be loaded with the maximum rated resistive current at the highest rated voltage for 3 hours at a rate no less than 1 operation per second, nor more than 30 operations per second. When applicable (see 3.1), the bias shall be applied at the rated value. The SSR shall be turned off 10 percent of the time and turned on 90 percent of the time. For single-pole double-throw and double-pole double-throw SSR's, cycling shall be 50 percent turned on and 50 percent turned off; or for 1.5 hours of test, 10 percent on and 90 percent off, and 90 percent on and 10 percent off for 1.5 hours of test.

4.7.2.6 Interim (pre-burn-in) electrical requirements (see 3.7.6). The interim (pre-burn-in) electrical requirements may be performed at the option of the manufacturer. Electrical parameters tested shall be those specified in 3.12, as applicable.

4.7.2.7 Burn-in test (see 3.7.7). Unless otherwise specified (see 3.1), SSR's shall be subjected to 160 hours +8 hours /-0 hours of operation at the maximum operating temperature. At the option of the manufacturer, the burn-in time-temperature regression table of MIL-STD-883,method 1015, may be used. Lower temperatures at higher load currents, in accordance with the specified derating curve, may be used with qualifying activity approval. Input and bias (where applicable) shall be at the rated ON state conditions. The output(s) shall be loaded with the maximum specified current derated for the test temperature. Output condition shall be monitored with latching failure circuitry and appropriate indicators. If scanning type condition monitoring is employed, each SSR shall be monitored at least once per second throughout the entire burn-in period.

Test conditions shall be measured on one randomly selected socket prior to start of the test. The values, the test temperature and start time shall be recorded on a burn-in log. At the completion of the test prior to removal of bias, the test conditions shall be measured on one randomly selected socket. The values, the temperature and the finish time shall be recorded on the burn-in log.

Any SSR's that fail during the burn-in shall be removed from the lot at the completion of burn-in. If the test conditions are interrupted for more than 10 minutes during the test (for example, due to equipment malfunction or power outages), the test duration shall be extended to ensure that actual exposure time is 160 hours +8 hours /-0 hours. Any such interruptions in the final eight hours of test shall require an extension of the test duration for eight hours following the last interruption.

4.7.3 Solderability (applicable to solder terminals) (see 3.8). SSR's shall be tested in accordance with method 208 of MIL-STD-202. All terminations of each SSR shall be tested.

4.7.4 Seal (see 3.9). SSR's shall be tested in accordance with 4.7.4.1 or 4.7.4.2 as applicable. In case of dispute, MIL-STD-883, method 1014, test condition A shall govern.

4.7.4.1 SSR's sealed with a tracer gas. SSR's sealed with a tracer gas shall be tested in accordance with method 112 of MIL-STD-202 (see 4.7.4.1a) or method 1014 of MIL-STD-883 (see 4.7.4.1b). The following details shall apply:

a. Method 112 of MIL-STD-202:

(1) Test condition C, procedure IV. SSR's shall be back filled with a helium tracer gas (90 percent dry gas and 10 percent helium). For gross leak, silicone oil shall not be used.

(2) Leakage rate sensitivity: 1×10^{-8} atm cm^3/s.

(3) Measurements after test: Not applicable.

b. Method 1014 of MIL-STD-883, test condition A or test condition B.

4.7.4.2 SSR's sealed without a tracer gas. SSR's sealed without a tracer gas shall be tested in accordance with method 1014 of MIL-STD-883. At the option of the manufacturer, either 4.7.4.2a or 4.7.4.2b may be used. The following details shall apply:

a. Method 1014 of MIL-STD-883:

(1) Test condition A1 or A2.

(2) Measurements after test: Perform a gross leak test in accordance with MIL-STD-202, method 112, test condition A, B, or D. Silicone oil shall not be used. At the option of the manufacturer, the gross leak test of MIL-STD-883, method 1014, test condition C, may be used.

b. Method 1014 of MIL-STD-883, test condition B.

4.7.4.3 Radioisotope dry gross leak test (optional). This test shall be used only to test SSR's that internally contain some krypton-85 absorbing medium, such as electrical insulation, organic sieve material, or molecular sieve material. This test shall be permitted only if the following requirements are met:

a. A 5 mil to 10 mil diameter hole shall be made in a representative unit of the SSR to be tested. (This is a one time test that remains in effect until a design change is made in the SSR internal technology.)

b. The SSR shall be subjected to this test condition. If the SSR exhibits a hard failure, this test condition may be used for those SSR's represented by the test unit. If the SSR does not fail, this test shall not be used and instead a +125°C fluorocarbon gross leak shall be performed in accordance with MIL-STD-202, method 112, test condition D, except the specimen shall be observed from the instant of immersion for 1 minute minimum to 3 minutes maximum.

4.7.4.3.1 Apparatus. The following apparatus shall be required for this test:

a. Radioactive tracer gas activation console containing krypton-85/dry nitrogen gas mixture.

b. Counting station with sufficient sensitivity to determine the radiation level of krypton-85 tracer gas inside the SSR.

c. Tracer gas mixture: Krypton-85/dry nitrogen with a minimum allowable specific activity of 100 microcuries per atmosphere cubic centimeter. The specific activity of the krypton-85/dry nitrogen mixture shall be a known value and determined on a once-a-month basis as a minimum.

4.7.4.3.2 Procedure. The SSR's shall be placed in a radioactive tracer gas activation tank and the tank shall be evacuated to a pressure not to exceed 0.5 torr. The SSR's shall then be subjected to a minimum of 10 pounds per square inch gage of krypton-85/dry nitrogen gas mixture for 30 seconds. The gas mixture shall then be evacuated in storage until a pressure of 2.0 torr maximum exists in the activation tank. The evacuation shall be completed in 5 minutes maximum. The evacuation tank shall then be backfilled with air (air wash). The SSR's shall then be removed from the activation tank and leak tested within 2 hours after gas exposure with a scintillation-crystal-equipped counting station. SSR's indicating 1,000 counts per minute or greater above the ambient background of the counting station shall be considered a gross leak failure.

4.7.5 Insulation resistance (see 3.10). SSR's shall be tested in accordance with method 1003 of MIL-STD-883. The following details and exceptions shall apply:

a. Test condition: E

b. Points of measurement:

(1) A common connection of each input circuit and every other isolated input circuit, if applicable.

(2) When specified (see 3.1), a common connection of all input terminals, and a common connection of all output terminals. Unless otherwise specified (see 3.1), the voltage shall be 500 volts, and the input shall be positive with respect to the output.

(3) A common connection of the terminals of each output pole, and a common connection of all other isolated output terminals.

c. Electrification time: 2 minutes, or until a stable reading is obtained.

4.7.6 DWV (see 3.11). SSR's shall be tested as specified in 4.7.6.1, and when specified (see 3.1), in accordance with 4.7.6.2.

NOTE: To avoid unnecessary failures, test voltages shall not be applied indiscriminately. Before beginning test, short-circuit connections shall be made between any set of non isolated input or output terminals in which there is a possibility that the SSR will be damaged if the test voltage is applied between them.

4.7.6.1 At atmospheric pressure. Solid state SSR's shall be tested in accordance with method 301 of MIL-STD-202. The following details shall apply:

a. Magnitude of test voltage: As specified (see 3.1).

b. Nature of potential: As specified (see 3.1).

c. Points of application: Chassis ground, if applicable, and a common connection of all other terminals.

d. Maximum leakage current: 1.0 mA.

e. Test time shall be 60 seconds for qualification testing and for all other testing at the specified dwv (see 3.1). If the test voltage is increased to 5 percent above the specified (see 3.1) voltage, the test time shall be 15 seconds.

f. Following these tests, SSR's shall be examined for evidence of arcing, flashover, insulation breakdown, and damage.

4.7.6.2 At reduced barometric pressure. SSR's specified (see 3.1) for operation above 10,000 feet shall be tested in accordance with method 105 of MIL-STD-202. The following details shall apply:

a. Method of mounting: Normal mounting means.

b. Test condition: C (unless otherwise specified) (see 3.1).

c. Tests during subjection to reduced pressure: As specified in 4.7.6.1, except test voltage shall be 1/3 of specified magnitude.

d. Same as 4.7.6.1e.

4.7.7 Electrical characteristics.

4.7.7.1 Reverse polarity (dc operated SSR's) (see 3.12.1).

a. Input configuration.

(1) Test setup per figure 1.

(2) Apply specified (see 3.1) load, voltage, and frequency (if applicable).

(3) Remove input voltage, and status voltage (if applicable), and reapply the specified (see 3.1) voltage in reverse polarity between input and input ground.

(4) Verify that the reverse input current (I(in)) is below the specified (see 3.1) value.

(5) Observe the output for any sign of turn-on by measuring V(output).

b. Control configuration.

(1) Test setup per figure 1.

(2) Apply specified (see 3.1) load, voltage, and frequency (if applicable).

(3) Remove all input voltages (bias, control, and status, if applicable). Apply the specified (see 3.1) voltage in reverse polarity between the specified (see 3.1) terminals.

(4) Verify that the reverse input current (I(in)) is below the specified (see 3.1) value.

(5) Observe the output for any sign of turn-on by measuring V(output).

4.7.7.2 Input Characteristics.

4.7.7.2.1 Input current (see 3.12.2).

a. Test setup per figure 1.

b. Apply maximum input voltage (V(in)).

c. Verify that input current (I(in)) is as specified (see 3.1).

4.7.7.2.2 Input turn-on voltage (see 3.12.3).

a. Test setup per figure 1.

b. Apply the specified (see 3.1) load, voltage, and frequency (if applicable).

c. Apply specified (see 3.1) input turn-on voltage (V(in)).

d. Verify that the SSR is ON by measuring the output current (I(output)) or by measuring output voltage drop (V(output)).

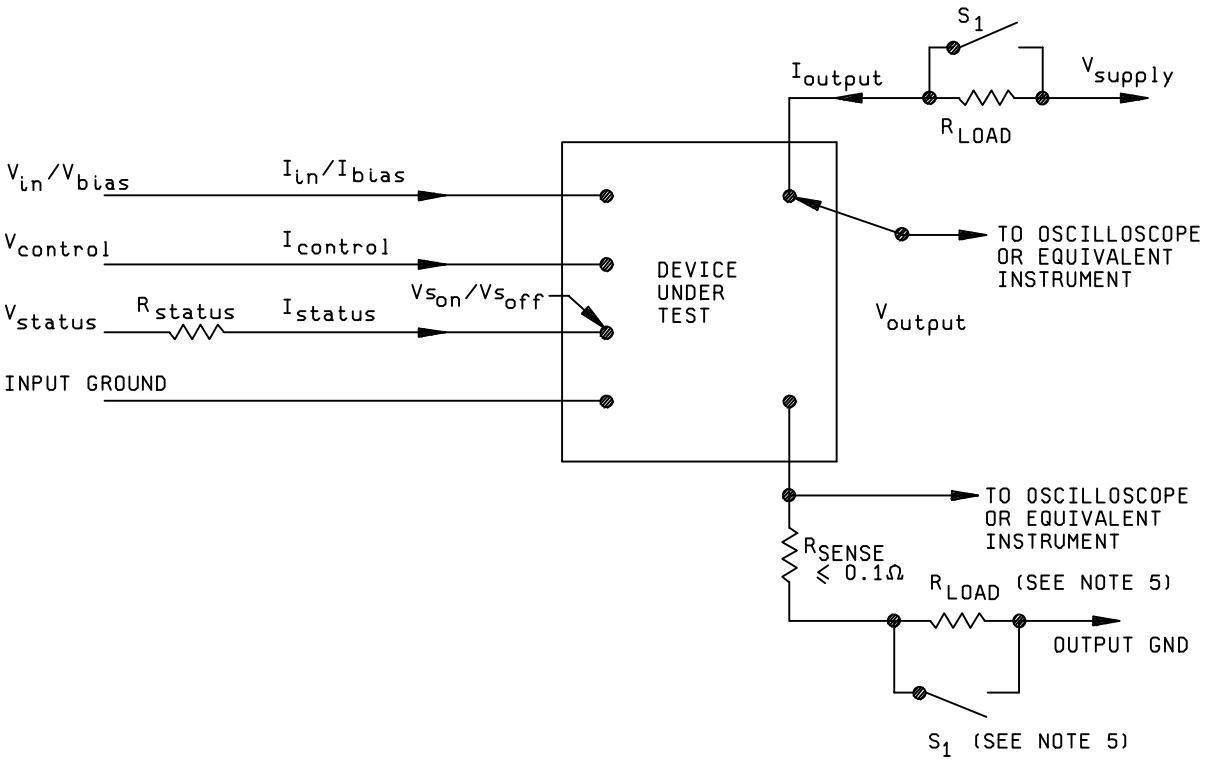
4.7.7.2.3 Input turn-off voltage (see 3.12.4).

a. Test setup per figure 1.

b. Apply specified (see 3.1) load, voltage and frequency (if applicable).

c. Apply specified (see 3.1) input turn-on voltage (V(in)) to turn the SSR ON. Then apply specified (see 3.1) input turn-off voltage (V(in)).

d. Verify that the SSR is OFF by measuring the output current (I(output)) to be within leakage current specification (see 3.1), or by measuring the output voltage (V(output)).



NOTES:

1. R_{SENSE} may be replaced by an isolated current probe (current transformers, hall effect devices, or equivalent).
2. Status terminals as applicable.
3. V_{STATUS} and R_{STATUS} as applicable.
4. Unless otherwise specified, resistive loads are used for testing methods.
5. Option load may be connected as shown.

FIGURE 1. General test setup.

4.7.7.2.4 Bias current (see 3.12.5).

a. Test setup per figure 1.

b. Apply maximum bias voltage, V(bias), then the specified (see 3.1) control voltage, V(control), to energize the bias current.

c. Verify that bias current (I(bias)) is as specified (see 3.1).

4.7.7.2.5 Control current (see 3.12.6).

a. Test setup per figure 1.

b. Apply specified (see 3.1) bias voltage, V(bias), and apply specified (see 3.1) control voltage, V(control).

c. Verify that control current, I(control), is as specification (see 3.1).

4.7.7.2.6 Control turn-on voltage (see 3.12.7).

a. Test setup per figure 1.

b. Apply the specified (see 3.1) load, voltage, and frequency (if applicable).

c. Apply the specified (see 3.1) bias voltage, V(bias), and the specified (see 3.1) Control Turn-On voltage, V(control) to turn the SSR on.

d. Verify that the SSR is ON by measuring the output current I(output), or by measuring output voltage drop V(output).

4.7.7.2.7 Control turn-off voltage (see 3.12.8).

a. Test setup per figure 1.

b. Apply the specified (see 3.1) load, voltage, and frequency (if applicable).

c. Apply the specified (see 3.1) bias voltage, V(bias), and control turn-on voltage to turn the SSR on. Then apply specified (see 3.1) control turn-off voltage to turn the SSR OFF.

d. Verify that the SSR is OFF by measuring the output current I(output) to be within leakage current specification (see 3.1), or by measuring the output voltage V(output).

4.7.7.3 Overload - will-not-trip current (see 3.12.9).

a. Test setup per figure 1.

b. Apply the specified (see 3.1) will-not-trip current, and frequency (if applicable).

c. Apply specified (see 3.1) input conditions for the specified (see 3.1) will-not-trip time.

d. Verify that the SSR remains ON for the specified (see 3.1) time by observing the output current, I(output), or the output voltage, V(output).

e. Verify that the SSR meets the trip characteristics at the various current levels specified (see 3.1).

4.7.7.4 Overload - must-trip current (see 3.12.10).

a. Test setup per figure 1.

b. Apply the specified (see 3.1) must-trip current, and frequency (if applicable).

c. Apply specified (see 3.1) input conditions for a time equal to or greater than the specified (see 3.1) must-trip time.

d. Verify that the SSR shuts OFF within the specified (see 3.1) time by measuring the output current, I(output), or the output voltage, V(output).

e. Verify that the SSR meets the trip characteristics at the various current levels specified (see 3.1).

4.7.7.5 Turn-on into a shorted load (see 3.12.11).

a. Test setup per figure 1.

b. Apply specified (see 3.1) voltage, and frequency (if applicable).

c. Close switch S1.

d. Apply specified (see 3.1) input conditions to turn the SSR on.

e. Verify that the SSR shuts OFF by measuring the output current I(output).

f. Reset SSR, then repeat twice the steps outlined in 4.7.7.5a through 4.7.7.5e. Repeating this turn-on into a shorted load test twice can be eliminated if the manufacturer has demonstrated process control under the SPC program (see 3.3.1), or other method that has been approved by the qualifying activity. If the design, material, technology, or processing of the part is changed or, if there are any quality problems or failures, the qualifying activity may require resumption of the specified testing. Deletion of testing does not relieve the manufacturer from meeting the test requirement in case of dispute.

4.7.7.6 Shorted load with SSR ON (see 3.12.12).

a. Test setup per figure 1.

b. Apply the specified (see 3.1) load, voltage, and frequency (if applicable).

c. Apply specified (see 3.1) input conditions to turn the SSR on.

d. Close switch S1.

e. Verify the SSR shuts OFF by measuring the output current I(output).

f. Reset SSR, then repeat twice the steps outlined in 4.7.7.6a through 4.7.7.6e. Repeating this shorted load test twice can be eliminated if the manufacturer has demonstrated process control under the SPC program (see 3.3.1), or other method that has been approved by the qualifying activity. If the design, material, technology, or processing of the part is changed or, if there are any quality problems or failures, the qualifying activity may require resumption of the specified testing. Deletion of testing does not relieve the manufacturer from meeting the test requirement in case of dispute.

4.7.7.7 Status turn-on time (see 3.12.13).

a. Test setup per figure 1.

b. Apply specified (see 3.1) load, voltage, and frequency (if applicable).

c. Apply specified (see 3.1) input conditions, and activate the necessary status conditions to turn the status output ON.

d. Verify that the status turn-on time is as specified (see 3.1).

4.7.7.8 Status "ON" voltage (see 3.12.14).

a. Test setup per figure 1.

b. Apply specified (see 3.1) load, voltage, and frequency (if applicable).

c. Apply specified (see 3.1) input conditions, and activate the necessary status conditions to turn the status output ON.

d. Verify that the status current, I(status), is as specified (see 3.1) and that the status "ON" voltage, V_s(on), is as specified (see 3.1).

4.7.7.9 Status turn-off time (see 3.12.15).

a. Test setup per figure 1.

b. Apply specified (see 3.1) load, voltage, and frequency (if applicable).

c. Apply specified (see 3.1) input conditions, and activate the necessary status conditions to turn the status output OFF.

d. Verify that the status turn-off time is as specified (see 3.1).

4.7.7.10 Status "OFF" voltage (see 3.12.16).

a. Test setup per figure 1.

b. Apply specified (see 3.1) load, voltage, and frequency (if applicable).

c. Apply specified (see 3.1) input conditions, and activate the necessary status conditions to turn the status output OFF.

d. Verify that the status current, I(status), is as specified (see 3.1) and that the status "OFF" voltage, V_s(off), is as specified (see 3.1).

4.7.7.11 Status blocking voltage (see 3.12.17).

a. Test setup per figure 1.

b. Apply specified (see 3.1) load, voltage, and frequency (if applicable).

c. Apply specified (see 3.1) input conditions and necessary status turn-off conditions.

d. Apply the specified (see 3.1) status blocking voltage, V(status).

e. Verify that the status current, I(status), is as specified (see 3.1).

4.7.7.12 Status leakage current (see 3.12.18).

a. Test setup per figure 1.

b. Apply specified (see 3.1) load, voltage, and frequency (if applicable).

c. Apply specified (see 3.1) input conditions and necessary status turn-off conditions.

d. Apply the maximum specified (see 3.1) status voltage, V(status),

e. Verify that the status leakage current, I(status), is as specified (see 3.1).

4.7.7.13 Turn-on time (see 3.12.19).

a. Test setup per figure 1.

b. Apply the specified (see 3.1) load, voltage, and frequency (if applicable).

c. Apply specified (see 3.1) input turn-on conditions.

d. Verify that the SSR turns ON in the specified (see 3.1) time by measuring the output voltage, V(output).

4.7.7.14 Turn-off time (see 3.12.20).

a. Test setup per figure 1.

b. Apply the specified (see 3.1) load, voltage, and frequency (if applicable).

c. Apply specified (see 3.1) input turn-on conditions, then apply the specified (see 3.1) input turn-off conditions.

d. Verify that the SSR turns OFF in the specified (see 3.1) time by measuring the output voltage V(output).

4.7.7.15 Output voltage drop (see 3.12.21).

a. Test setup per figure 1.

b. Apply the specified (see 3.1) load, voltage, and frequency (if applicable).

c. Apply specified (see 3.1) input turn-on conditions.

d. Verify that the voltage drop is as specified (see 3.1) by measuring V(output).

4.7.7.16 Output leakage current (see 3.12.22).

a. Test setup per figure 1.

b. Apply the specified (see 3.1) load, voltage, and frequency (if applicable).

c. Apply the necessary input conditions to turn the output off.

d. Verify leakage current is as specified (see 3.1) by measuring I(output).

4.7.7.17 Transient voltage (see 3.12.23).

a. Test setup per figure 1.

b. Apply the necessary input conditions to turn the output off.

c. Apply the specified (see 3.1) voltage, and frequency (if applicable), and test load.

d. For the specified (see 3.1) time apply the specified (see 3.1) transient voltage to the output of the SSR. For the purpose of test, a low current supply may be used.

e. Monitor the output to verify that the SSR does not turn on.

4.7.7.18 DC offset voltage (ac SSR's only) (see 3.12.24).

a. Test setup per figure 2.

b. Apply the specified (see 3.1) load, voltage, and frequency.

c. Apply specified (see 3.1) input turn-on conditions.

d. Verify the offset voltage is as specified (see 3.1) by measuring V(offset).

4.7.7.19 Waveform distortion (ac SSR's only) (see 3.12.25).

a. Test setup per figure 1.

b. Apply specified (see 3.1) load, voltage and frequency.

c. Apply specified (see 3.1) input turn-on conditions.

d. With SSR turned ON, verify that output voltage, V(output), is as specified (see 3.1) (see figure 3).

4.7.7.20 Minimum load current rating (ac SSR's only) (see 3.12.26).

a. Test setup per figure 1.

b. Apply specified (see 3.1) voltage and frequency, and minimum specified (see 3.1) load current.

c. Apply specified (see 3.1) input turn-on conditions.

d. Verify that the SSR turns ON and remains ON by measuring the output voltage, V(output).

4.7.7.21 Exponential rate of voltage rise (dv/dt) (see 3.12.27).

a. Test setup per figure 4, or equivalent as approved by the qualifying activity.

b. Apply zero bias voltage (if applicable) and zero control voltage.

c. Connect the output terminals of the SSR under test to the circuit of figure 4.

d. Close and open S1 for a minimum of 10 times. After 5 cycles, reverse the polarity to the SSR (ac SSR's only). Verify that the SSR achieves the specified (see 3.1) output voltage within the specified (see 3.1) time by measuring V(output).

4.7.7.22 Zero Crossing (ac SSR's only) (see 3.12.28).

a. Test setup per figure 1.

b. Apply specified (see 3.1) load, voltage and frequency.

c. Apply specified (see 3.1) input turn-on conditions.

d. Apply the input turn-on condition at 90°(±10°) and 270° (±10°) of the load supply voltage and monitor the output voltage waveform, V(output), for the moment of turn-on. The maximum value of "zero" voltage turn-on shall be as specified (see 3.1).

e. Apply the input turn-off condition at 90°(±10°) and 270° (±10°) of the load supply voltage and monitor the output current waveform, I(output), for the moment of turn-off. The SSR shall not turn off with the removal of input conditions until the ac load current is below the specified (see 3.1) value.

4.7.7.23 Electrical system spike, 25°C only. (see 3.12.29) (for qualification and periodic inspections only).

a. Test setup per figure 5.

b. With switch S3 open and switch S2 closed, cycle switch S1 and observe oscilloscope CH1 (or other equivalent instrument). Adjust V1 to obtain a minimum spike amplitude of 600 volts.

c. Close switch S3 and cycle switch S1 at 10 pulses ±1 pulse per second for the specified (see 3.1) time.

d. Reverse the polarity of V1 and repeat 4.7.7.23b and 4.7.7.23c.

e. After completion, the SSR shall be tested for output leakage current (4.7.7.16), turn-on time (4.7.7.13), and turn-off time (4.7.7.14).

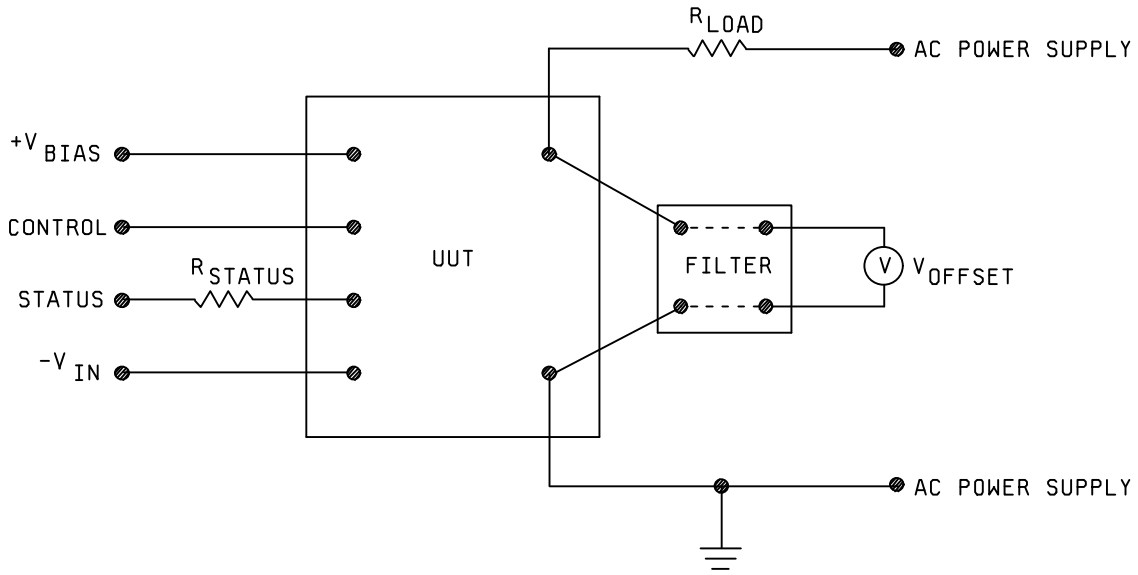
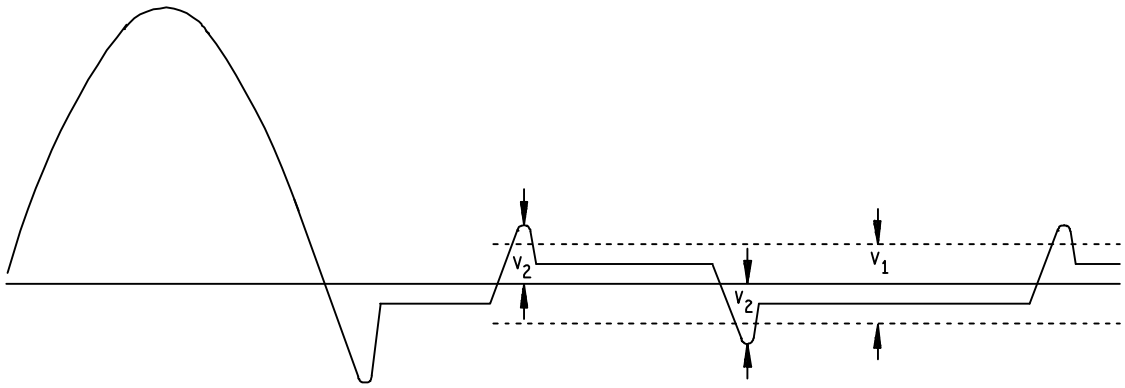


FIGURE 2. dc offset voltage setup.

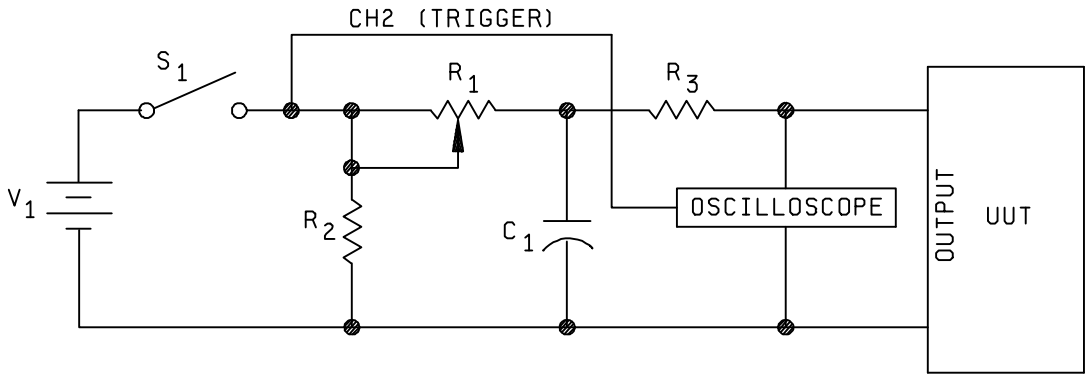


V_1 = WAVEFORM DISTORTION VOLTAGE (RMS)

V_2 = WAVEFORM DISTORTION VOLTAGE (PEAK)

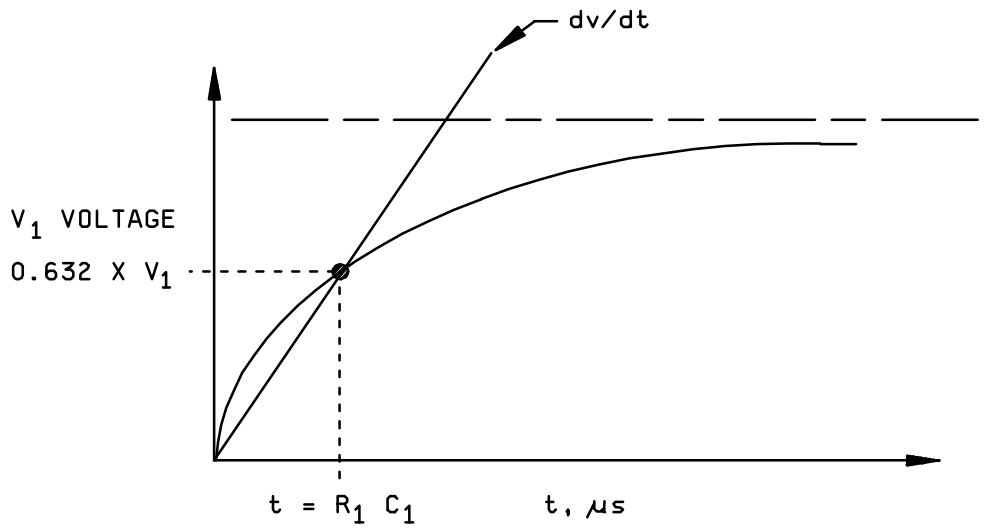
1

FIGURE 3. Waveform distortion.



V_1 = Maximum rated output voltage (ac devices use $V_1 = V_{RATED}$ (RMS) x 1.414).
R_1 = See equation below.
R_2 = 1.0 megohm (±5 percent), 1/2 watt.
R_3 = 50 ohm (±5 percent).
C_1 = 0.01 mF (±5 percent).
S_1 = 10 amp Hg wetted switch (or equivalent).

DV/DT test setup



DV/DT curve

FIGURE 4. DV/DT.

4.7.7.24 Overload, 25°C only. (see 3.12.30) (for qualification and periodic inspections only).

a. Test setup per figure 1.

b. Apply the specified (see 3.1) overload conditions. Unless otherwise specified (see 3.1), the load shall be 3.5 times the specified (see 3.1) current at specified (see 3.1) voltage.

c. Apply specified (see 3.1) input turn-on conditions.

d. The SSR's shall be cycled on and off 10 times. The period shall be 1 second and the duty cycle shall be 10 percent, unless otherwise specified (see 3.1).

e. After completion, the SSR shall be tested for output leakage current (4.7.7.16), and turn-on voltage in accordance with 4.7.7.2.2 or 4.7.7.2.6 as applicable.

4.7.7.25 Power dissipation, 25°C only. (see 3.12.31) (for qualification inspections and periodic inspections only).

a. ON state:

(1) Test setup per figure 1.

(2) Apply the maximum load, voltage, and specified frequency (if applicable).

(3) Apply specified (see 3.1) maximum input turn-on conditions.

(4) Measure all currents and corresponding voltages and calculate the product of each. Calculate the power dissipation by adding each product with the output voltage drop times output current, for each output switch in addition to any power dissipated by internal power supplies.

(5) Verify that the total power dissipation does not exceed the specified (see 3.1) limits.

b. OFF state:

(1) Test setup per figure 1.

(2) Apply the maximum load, voltage, and specified frequency (if applicable).

(3) Apply specified (see 3.1) maximum input turn-off conditions.

(4) Measure all currents and corresponding voltages and calculate the product of each. Calculate the power dissipation by adding each product with the output voltage drop times output current, for each output switch in addition to any power dissipated by internal power supplies.

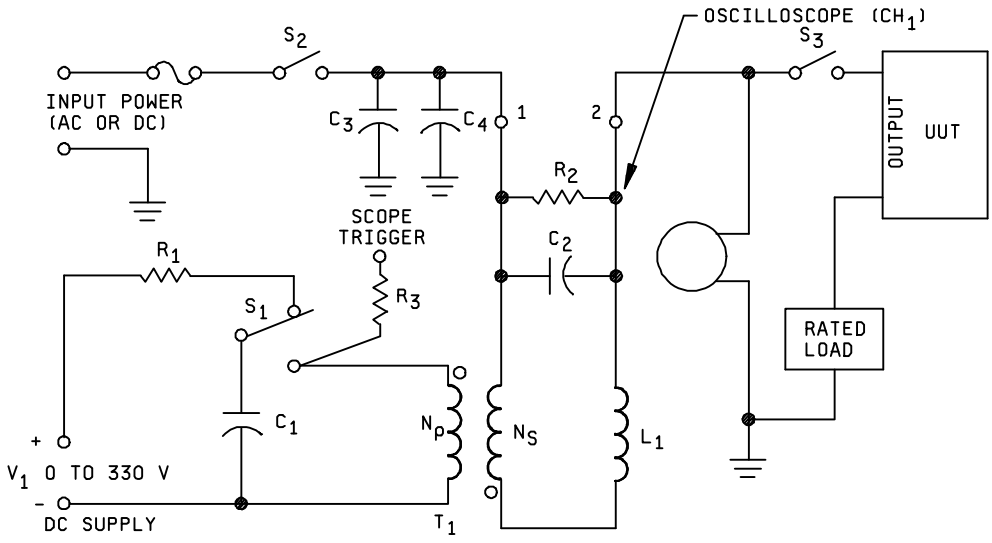
(5) Verify that the total power dissipation does not exceed the specified (see 3.1) limits.

4.7.8 Resistance to solvents (see 3.13). SSR's shall be tested in accordance with method 215 of MIL-STD-202 or method 2015 of MIL-STD-883. The following details and exceptions shall apply:

a. Portion to be brushed: All marking.

b. Specimens to be tested: One specimen each for the four solutions.

c. Examination: Specimens shall be examined for legibility of marking.



NOTES:

1. A mechanically or electronically operated switch may be used to replace S1.
2. The transformer windings should be bi-fillar.
3. A 50 ohm resistor replaces the equipment under test for verifying the source impedance.
4. Component values are as follows:

C_1	=	2 microfarads, 1500 volts
C_2	=	0.03 microfarads, 2000 volts
C_3	=	10 microfarads, 1000 volts
C_4	=	0.01 microfarads, 1000 volts
R_1 and R_2	=	100 ohms, 1 watt
R_3	=	1 megohm, 0.5 watt
S_1, S_2, and S_3	=	20 amp, SPDT switch
L_1	=	50 turns, 2 inch diameter/ #16 AWG
T_1	=	Air core transformer, 2 inch diameter/ #16 AWG Np = 20 turns, Ns = 60 turns

FIGURE 5. Electrical system spike test setup.

4.7.9 Shock (specified pulse) (see 3.14). SSR's shall be tested in accordance with method 213 of MIL-STD-202. The following details and exceptions shall apply:

a. Mounting method: As specified in 4.7.10b.

b. Test condition: F.

c. Electrical power shall not be applied to the SSR during this test.

d. Measurements and examinations after shock: As specified in 4.7.10e.

4.7.10 Vibration (see 3.15). SSR's shall be tested in accordance with method 204 of MIL-STD-202. The following details and exceptions shall apply:

a. Tests and measurements prior to vibration: None.

b. Method of mounting: Rigidly mounted by normal mounting means. SSR's designed for printed-circuit board application shall be soldered by normal means to a printed-circuit board of any convenient size, which shall in turn be secured by screws to a suitable fixture.

c. Test condition: F, except 100 gravity units (g's) peak.

d. Electrical power will not be applied to the SSR during this test.

e. Measurements and examination: SSR's shall then be examined for evidence of breaking, cracking, chipping or flaking of the finish, or loosening of the terminals.

4.7.11 Terminal strength (see 3.16). SSR's shall be tested in accordance with method 211 of MIL-STD-202 in accordance with the following, as applicable. Unless otherwise specified herein, two terminals of each discrete design, size, and configuration shall be tested; however, if there is only one terminal of such design, size, and configuration, it shall be tested.

4.7.11.1 Pull test (all terminal types). Terminals shall be tested as specified in MIL-STD-202, method 211, test condition A. The force shall be as specified (see 3.1).

4.7.11.2 Bend test (not applicable to plug-in terminals). Terminals shall be tested as specified in MIL-STD-202, method 211, test condition B (two bends) or test condition C, as applicable. Loads for test condition C shall be as specified (see 3.1).

4.7.11.3 Twist test (wire-lead terminals only). All terminals shall be tested as specified in MIL-STD-202, method 211, test condition D except during application of torsion, each terminal shall be rotated 45 degrees in one direction, then returned to start; rotated in opposite direction 45 degrees, then returned to start. Each terminal shall be subjected to two such rotations and returns. Each terminal shall be held at a point 0.25 inch from the point of emergence from the SSR and in one plane shall be bent 20 degrees ±5 degrees in one direction, then returned to start; rotated in opposite direction 20 degrees ±5 degrees, then returned to start. This procedure shall then be repeated in the perpendicular plane. Following these tests, SSR's shall be examined for evidence of loosening or breaking of the terminals and other damage that could adversely affect the normal operation of the SSR.

4.7.12 Moisture resistance (applicable to nonhermetically sealed SSR's only) (see 3.17). SSR's shall be tested in accordance with method 106 of MIL-STD-202. The following details and exceptions shall apply:

a. Mounting: On a corrosion-resistant panel by normal mounting means.

b. Initial measurement: Not applicable.

c. Polarization: During steps 1 through 6, 100 volts shall be applied between the input (positive) and the case, frame, or enclosure (negative), as applicable on one half of the sample SSR's. No polarization voltage shall be applied to the other half of the sample SSR's.

d. Final measurements: Upon completion of step 6 of the final cycle, insulation resistance shall be measured as specified in 4.7.5. After a 24-hour drying period at a relative humidity of 50 percent ±5 percent, DWV shall be measured as specified in 4.7.6, except the test voltage shall be 90 percent of initial potential.

e. Examination after test: SSR's shall be examined for evidence of breaking, cracking, chipping or flaking of the finish, or loosening of the terminals.

4.7.13 Crosstalk (when specified) (see 3.18). Crosstalk shall be measured using equipment which shall have an input impedance of 1 megohm, minimum, and shall be paralleled with a capacitance of 20 picofarads maximum. A 1.0 to 10.0 volts peak-to-peak input signal at frequencies up to 10 megahertz shall be applied to the switching circuit through coaxial cable, terminated in 50 ohms ±5 percent at the SSR terminal. The coaxial cable shall conform to MIL-C-17. The input signal amplitude shall be measured at the terminals of the SSR. The terminals where crosstalk is to be detected shall be connected through a similar type coaxial cable, terminated in 50 ohms ±5 percent at the measuring SSR. The resultant attenuation, in decibels, equals:

$$20 * (\mathrm{Log}_{10} V_{in} / V_{out})$$

4.7.14 Isolation (when specified) (see 3.19). The capacitance shall be measured using method 305 of MIL-STD-202. The following details apply:

a. Test frequency: 1 kilohertz (kHz).

b. Points of measurement: Between all isolated terminals.

4.7.15 Resistance to soldering heat (when specified) (see 3.20). SSR's shall be tested in accordance with method 210 of MIL-STD-202. The following details and exceptions shall apply:

a. Depth of immersion in molten solder: Within .060 inch ±.020 inch of the SSR base.

b. Test condition: B.

c. Measurements after test: Insulation resistance and DWV as specified in 4.7.5 and 4.7.6.

d. Examination after test: As specified in 4.7.12e.

4.7.16 Salt atmosphere (corrosion) (see 3.21). SSR's shall be tested as specified in 4.7.16.1 or, when specified (see 3.1), in accordance with 4.7.16.2.

4.7.16.1 Salt atmosphere (corrosion), (when specified, see 3.1). SSR's shall be tested in accordance with method 1041 of MIL-STD-750. Examination after test shall be as specified in 4.7.16.2c.

4.7.16.2 Salt spray. SSR's shall be tested in accordance with method 101 of MIL-STD-202. The following details and exceptions shall apply:

a. Applicable salt solution: 5 percent.

b. Test condition: B.

c. Examination after test: SSR's shall be examined for evidence of peeling, chipping, or blistering of the finish, and exposure of base metal due to corrosion.

4.7.17 Life (see 3.22). SSR's shall be subjected to the following procedures:

a. With the SSR's mounted in accordance with 4.7.10b, they shall be operated for 48 hours in accordance with 4.7.2.5, except the duration of the turn-on shall be 50 percent ±5 percent of each operation of the SSR. The ambient temperature of the SSR environment shall be maintained at the highest specified operating temperature (see 3.1). Repeat as above for 48 hours, except with the ambient temperature at the lowest specified operating temperature. Repeat as above for 48 hours, except with the temperature at room ambient.

b. Same as 4.7.17a, except with the maximum turn-off voltage continuously applied to the input. SSR's shall be monitored to verify that they remain turned off.

c. Same as 4.7.17b, except with the minimum turn-on voltage continuously applied to the input. SSR's shall be monitored to verify that they remain turned on.

d. The transient voltage test shall then be performed as specified in 4.7.7.17.

e. Repeat steps 4.7.17a through 4.7.17d for each additional load specified.

f. After the above tests, SSR's shall be subjected to the insulation resistance, DWV, and the electrical characteristics (see 4.7.5, 4.7.6, and 4.7.7.1 through 4.7.11).

5. PACKAGING

5.1 Packaging. For acquisition purposes, the packaging requirements shall be as specified in the contract or order (see 6.2). When actual packaging of materiel is to be performed by DoD personnel, these personnel need to contact the responsible packaging activity to ascertain requisite packaging requirements. Packaging requirements are maintained by the Inventory Control Point's packaging activity within the Military Department or Defense Agency, or within the Military Department's System Command. Packaging data retrieval is available from the managing Military Department's or Defense Agency's automated packaging files, CD-ROM products, or by contacting the responsible packaging activity.

6. NOTES

(This section contains information of a general or explanatory nature that may be helpful, but is not mandatory.)

6.1 Intended use. SSR's conforming to this specification are intended for use in communication, radar, digital control, and other electronic systems. Their principle areas of application are for aircraft, missiles, spacecraft, shipboard, and ground-support equipment. SSR's covered by this specification shall be able to operate satisfactorily in systems under the following demanding conditions: operating temperature range of -55°C to +125°C, 20 g's to 100 g's of vibration, 50 g's to 1500 g's of shock, up to 5000 g's of acceleration, and have reduced susceptibility to corrosion in salt water environments. These requirements are verified under a qualification system.

CAUTION: Users are cautioned to ensure that temperature limitations, transient voltages and momentary current overloads do not exceed the applicable parameters of a SSR proposed for a specific application. During high voltage testing, due caution should be exercised to avoid damage. Polarity, when applicable, should be observed. Due to the use of nonlinear-response assembly parts and the inherent difference between electromechanical and SSR's, output impedance values for like rated electromechanical relays and SSR's are not necessarily the same.

6.2 Acquisition requirements. Acquisition documents should specify the following:

a. Title, number, and date of the specification.

b. Title, number, and date of the applicable specification sheet, and the part number.

c. Issue of DoDISS to be cited in the solicitation, and if required, the specific issue of individuals documents referenced (see 2.2 and 2.3)

d. Packaging requirements (see 5.1)

6.3 Qualification. With respect to products requiring qualification, awards will be made only for products which are, at the time of award of contract, qualified for inclusion in Qualified Products List whether or not such products have actually been so listed by that date. The attention of the contractors is called to these requirements, and manufacturers are urged to arrange to have the products that they propose to offer to the Federal Government tested for qualification in order that they may be eligible to be awarded contracts or orders for the products covered by this specification. Information pertaining to qualification of products may be obtained from Defense Supply Center, Columbus, ATTN: DSCC-VQP, 3990 East Broad Street, Columbus, Ohio, 43213-1199.

6.4 Definitions. The definitions listed below are not a complete glossary of SSR terminology, but are definitions of the technical terms as applied in this specification.

a. Assured turn-off voltage. The assured turn-off voltage is the maximum value of the input voltage at which the SSR is guaranteed to turn off.

b. Assured turn-on voltage. The assured turn-on voltage is the minimum value of the input voltage at which the SSR is guaranteed to turn on.

c. Bias current. The bias current is required in SSR's with single or multiple double throw outputs to energize the normally closed switches when this current is not obtained from the load side of the SSR. A bias current is also required in special SSR designs such as an electronic latching relay.

d. Bias voltage. Bias voltage is a voltage that is always present at the input of the SSR. This voltage provides steady state current to the electronics in the input circuit of the SSR. The bias voltage does not control the state of the output of the SSR. (See control configuration, 6.4e).

e. Control configuration. Control configuration requires a bias voltage present, and a separate “control” input. This “control” input determines the state of the output of the SSR.

f. DC offset voltage. AC SSR's use semiconductors which switch each half cycle of the supply voltage independently. Consequently, a dc component of voltage can be developed as a result of unsymmetrical switching and unbalance in voltage drop across each semiconductor switch. This is detrimental to loads, such as transformers, if the dc component of voltage is excessive.

g. Heat sink. A heat sink is a device to which the SSR is attached for the purpose of conducting, absorbing, and radiating heat away from the SSR so that its case temperature is not exceeded. Heat sinks may also be attached to high power dissipating devices within the SSR to aid in the transfer of heat from the device to the case of the SSR.

h. Input. The circuitry within a SSR which responds to input voltage and causes the SSR to turn on.

i. Input configuration. Input configuration requires only one voltage (or current) applied at the input terminals. This input voltage determines the state of the output of the SSR.

j. Load current. Load current is the intended maximum current the SSR is capable of carrying for an indefinite amount of time.

k. Output. The circuit within a SSR which changes from conducting to nonconducting state and vice-versa.

l. Reset. The restoration of the tripped SSR to a state from which it can be turned on.

m. Reverse polarity protection (dc operated SSR's only). An input circuit that prevents damage to the SSR, limits the input current and prevents SSR turn-on when the input terminals are inadvertently reversed.

n. Short circuit protected SSR. A SSR with circuit breaker type action that protects the SSR from overload, shorted load or over-temperature conditions.

o. SSR. A static relay or relay unit constructed exclusively of solid state components. See MIL-R-28776 for hybrid relays.

p. Status. An auxiliary, low-current switch segment of the SSR that indicates the condition of the SSR. Examples of status are switch status (main switch open or closed); trip status (main switch turned off due to overcurrent); flow status (minimum output current flowing); and B.I.T (built-in-test).

q. Time, turn-off. The interval between the removal of input voltage and the output reaching 90 percent of its ultimate change in voltage when the SSR is turned off.

r. Time, turn-on. The interval between the application of input voltage and the output reaching 90 percent of its ultimate change in voltage when the SSR is turned on.

s. Trip. The automatic interruption of current which results from electrical overloads.

t. Trip curve. The trip curve sets the minimum and maximum trip points of the SSR and is plotted as current versus time, typically an inverse I^2t relationship.

u. Turn-on. The change in SSR condition (caused by the input voltage exceeding a predetermined minimum turn-on voltage) resulting in the output changing from a nonconducting to a conducting state (or vice-versa).

v. Waveform distortion. Improper silicon controlled rectifier gating circuit design can result in deviation from the fundamental sinusoidal current or voltage waveform.

w. Zero crossover (ac SSR's only). A desirable characteristic in SSR's that switch ac voltages. This characteristic is designed into the SSR to force it to turn on only near zero voltage and to turn off near zero load current in the ac voltage and current cycles when connected in series with the load regardless of when the input voltage is applied or removed. This design feature is beneficial in extending SSR life while reducing radiated electromagnetic interference.

6.5 Application information. SSR's enjoy the advantages of sensitivity, bounce-free contact action, and indefinitely long life in environments which do not exceed the voltage or temperature rating.

6.5.1 SSR/mounting surface interface. The interface between the SSR and its mounting surface should be given special attention because most of the heat generated within the SSR shall pass through this interface. To insure that this interface passes as much heat energy as possible, while remaining relatively cool, the thermal resistance (degree Celsius rise per watt dissipated within the SSR) between the SSR case and the mounting surface (especially for load currents over 1.0 ampere) should be kept as low as possible.

6.6 Guidance documentation.

6.6.1 Lead and terminal material. The following lead and terminal materials should be considered for meeting the performance requirements of this specification (see 3.6.11.1):

a. Type A: Iron-Nickel-Cobalt alloy: MIL-I-23011, class I, ASTM F15.

b. Type B: Iron-Nickel alloy (41 percent Ni): MIL-I-23011, class 5, ASTM F30.

c. Type C: Co-fired metallization such as nominally pure tungsten. The composition and application processing of these materials should be subject to qualifying activity approval.

d. Type D: Copper core-iron nickel ASTM F30 alloy (50.5 percent Ni). The core material should consist of copper (oxygen-free) ASTM B170, grade 2.

e. Type E: Copper core ASTM F15 alloy. The core material should consist of copper (oxygen-free) ASTM B170, grade 2.

f. Type F: Copper (oxygen free) ASTM B170, grade 2. This material should not be used as an element of any glass-to-metal seal structure.

g. Type G: Iron-Nickel alloy (50.5 percent Ni): MIL-I-23011, class 2 ASTM F30.

6.6.2 Lead finish. The following lead finishes should be considered for meeting the performance requirements of this specification:

a. Hot solder dip. The hot solder dip should be homogeneous with a minimum thickness of 60 microinches (1.52 μm) for round leads and, for other shapes, a minimum thickness at the crest of the major flats of 200 microinches (5.08 μm) solder (SN60 or Sn63). In all cases, the solder dip should extend up to and beyond the effective seating plane for packages with standoffs or within .030 inch (0.76 mm) of the lead or package interface for leaded flush mounted SSR's. For leadless chip carrier SSR's, the hot solder dip should cover a minimum of 95 percent of the metallized side castellation or notch and metallized areas above and below the notch except the index feature if not connected to the castellation. Terminal area intended for SSR mounting should be completely covered. The hot solder dip is applicable:

(1) Over a finish in accordance with entry 6.6.2b or 6.6.2c below, or

(2) Over electroplated nickel or electroless nickel phosphorous (see 6.6.3), or

(3) Over the basis metal. When applied over the basis metal, underplate that is nonconforming, or other finishes that are nonconforming (e.g., fused tin less than 200 microinches), hot solder dip should cover the entire lead to the glass seal or point of emergence of the lead or metallized contact through the package wall.

b. Tin-lead plate. Tin-lead plating should have in the plated deposit 3 percent to 50 percent by weight lead (balance nominally tin) homogeneously co-deposited. As plated tin-lead should be a minimum of 300 microinches thick. As plated tin-lead should contain no more than 0.05 percent by weight
co-deposited organic material measured as elemental carbon. Tin-lead plate is applicable:

(1) Over electroplated nickel or electroless nickel phosphorous in accordance with 6.6.3.

(2) Over the basis metal.

c. Gold plate. Gold plating should be a minimum of 99.7 percent gold, and only cobalt should be used as the hardener. Gold plating should be a minimum of 50 microinches (1.27 μm) and a maximum of 225 microinches (5.72 μm) thick. Gold plating should be permitted only over nickel plate or undercoating in accordance with 3.6.11.4.

6.6.3 Nickel plate or undercoating. Electroplated nickel undercoating or finishes from a sulfamate nickel bath is preferred and should be 50 microinches to 350 microinches (1.27 μm to 8.89 μm) thick measured on major flats or diameters. Electroless nickel undercoating or finishes, when allowed, should be 50 microinches to 350 microinches (1.27 μm to 8.89 μm) thick measured on major flats or diameters. The addition of organic "wetting agents" is prohibited for either sulfamate or phosphorous nickel baths. Electroplate or electroless nickel plate (or combinations thereof) as well as nickel cladding may be used as the finish for package elements other than flexible leads or terminals provided the corrosion resistance and environmental requirements are met. In all cases, electroplated nickel undercoating from a nickel sulfamate bath is preferred for lead finishes. Electroless nickel should not be used as the undercoating on flexible or semiflexible leads (see 3.3.1 and 3.3.2 of method 2004 of MIL-STD-883) and should be permitted only on rigid leads or package elements other than leads.

6.6.4 Solder dip (retinning) leads. Only the manufacturer, at their option, may solder dip/retin the leads of the product supplied to this specification provided the solder dip/retin process has been approved by the qualifying activity.

6.7 Sealing (degassing). The following procedure is suggested as a guide; however, every effort should be made to utilize the most effective procedure consistent with the state of the art.

a. Evacuate to less than 200 micrometers.

b. Heat to maximum rated ambient temperature with continued evacuation (see 3.1).

c. Maintain heat and vacuum for 12 hours or longer, continuing the treatment until a maximum pressure of 80 micrometers is reached.

d. Turn off heaters and maintain pressure for four hours.

e. Close evacuation valve and fill chamber with the desired inert pressurizing gas.

f. Seal SSR before removing from chamber.

6.8 PIN. This specification requires a PIN that describes technology and appropriate references to associated documents (see 1.3 and 3.1).

6.9 Subject term (key word) listing.

a. Bias input configuration

b. Control input configuration

c. Hybrid

d. Marking

e. Relay, solid state

f. Screening

g. Short circuit protection

6.10 Changes from previous issue. Marginal notations are not used in this revision to identify changes with respect to the previous issue due to the extensiveness of the changes.

APPENDIX A

CLASS II SOLID STATE RELAY QPL SYSTEM REQUIREMENTS

A.1 SCOPE

A.1.1 Scope. This appendix establishes additional requirements for the QPL system for class II SSR's. The manufacturer shall maintain and demonstrate this system to the qualifying activity as prerequisite for qualification and retention of qualification. This system shall be part of the overall QPL system under MIL-STD-790. Appendix A is a mandatory part of the specification. The information contained herein is intended for compliance.

A.2 APPLICABLE DOCUMENTS

SPECIFICATIONS

DEPARTMENT OF DEFENSE

MIL-PRF-38534 - Hybrid Microcircuits, General Specification for.

STANDARDS

DEPARTMENT OF DEFENSE

MIL-STD-883 - Test Methods and Procedures for Microelectronics.

MIL-STD-1276 - Leads for Electronic Component Parts.

A.3 REQUIREMENTS

A.3.1 Design, processing, manufacturing equipment, and materials instructions. SSR design, processing, manufacturing equipment and materials shall be documented in drawings, standards, specifications, or other appropriate media which shall cover the requirements and tolerances for all aspects of design and manufacturing including equipment test and prove-in, materials acquisition and handling, design verification testing and processing steps. As a minimum requirement, detailed documentation shall exist for the following items and shall be adequate to assure that quantitative controls are exercised, that tolerances or limits of control are sufficiently tight to assure a reproducible high quality product and that process and inspection records reflect the results actually achieved:

a. Incoming materials control (substrates, packages, active and passive chips or elements, wire, water purification, etc.).

b. Masking, photoresist, and mask registration.

c. Glassivation or passivation.

d. Metallization and film deposition.

e. Die, element, or substrate attachment.

f. Wire bonding.

g. Rework.

h. Sealing.

A.3.2 Cleanliness and atmosphere control in work areas. The requirements for cleanliness and atmosphere control in each work area in which unsealed SSR's, or parts thereof, are processed or assembled shall be documented. The manufacturer shall establish action and absolute control limits (at which point work stops until corrective action is completed) based on historical data and criticalness of the process in each particular area. For foreign material identification and control, see internal visual inspection requirements of MIL-STD-883, method 2017.

A.3.3 Environment control. The following are minimum environmental control requirements. All fabrication, assembly, and testing of class II SSR's prior to preseal visual shall be in an environment meeting class 100,000 particle count requirements, except soldering operations may be performed outside this environment and shall be approved by the qualifying activity. SSR's awaiting preseal visual inspection; SSR's accepted at preseal visual inspection and awaiting further processing; and noncontinuous production lots accumulated after element attach and prior to preseal visual (including SSR's delidded for rework or repair) shall be stored in a dry nitrogen environment. (Noncontinuous production shall occur when SSR's are held by the manufacturer, with no additional assembly work performed, for more than 30 days). The preseal visual inspection and the preparation for sealing environment shall be in accordance with MIL-STD-883, method 2017 and method 2032.

A.3.4 Rework and repair provisions. All rework and repair permitted on SSR's shall be as specified herein. This documentation shall reflect the processes, procedures, and materials to be used including verification or test data, and be approved by the qualifying activity of this specification. Each process or procedure shall be designated as rework or repair. This documentation shall indicate that a decision to rework is made solely by the manufacturer while a repair decision shall be made with the concurrence of the qualifying activity except for repairs permitted by this specification. A typical example of rework is the removal of a defective element and replacement with a new element. An example of repair is the use of an organically attached molytab to replace a previously alloy attached semiconductor element.

A.3.4.1 General rework and repair provisions.

a. All temperature excursions during any rework or repair shall not exceed the baselined rework or repair limitations. Time and temperature limits shall be specified.

b. Touch-up of package sealing surface plating on delidded packages is not permitted. Package sealing surface plating shall not be replated on delidded packages.

c. The minimum distance between the glass to metal seals and the package sealing surface shall be at least 0.040 inch (1.02 mm) after final seal to prevent damage to lead seals by welding adjacent to them. (Applies to seam welding only.)

d. Any SSR which is reworked or repaired after preseal visual inspection shall be subjected to full screening or rescreening as applicable. If a SSR has not been subjected to a given required screen prior to rework or repair, then that SSR shall be subjected to that screen after repair or rework. If a SSR has been subjected to a given screen prior to rework or repair, then rescreening applies as follows:

(1) Preseal visual inspection. Inspection for general damage (low magnification in accordance with MIL-STD-883, method 2017 and method 2032) which might have been caused by the rework or repair. Perform a complete method 2017 or method 2032 inspection of the reworked or repaired element or area (e.g., replaced die, wire bonds, etc.).

(2) Stabilization bake, temperature cycle or thermal shock, mechanical shock, constant acceleration, seal, and external visual. Rescreen all reworked or repaired SSR's 100 percent.

(3) Burn-in. SSR's delidded to rework package seal failures do not require burn-in rescreen. SSR's which have had elements replaced or have been wire bonded or rewirebonded require 100 percent burn-in rescreen.

e. When flux is required for rework or repair, the specific flux and detailed procedures for its use and subsequent special cleaning operations shall be documented and approved in accordance with A.3.1.

f. Replacement elements shall not be bonded onto the chip element they are to replace.

A.3.4.2 Element wire rebonding. Wire rebonding of elements other than substrates shall be permitted with the following limitations:

a. No scratched, voided, or discontinuous paths or conductor patterns on an element shall be repaired by bridging with bonding wire or ribbon, or by the addition of bonding wire or ribbon.

b. All rebonds shall be placed on at least 50 percent undisturbed metal (excluding probe marks that do not expose underlying oxide). No more than one rebond attempt at any design bond location shall be permitted. No rebonds shall touch an area of exposed oxide caused by lifted or blistered metal. A bond shall be defined as a wire to post or wire to pad bond. Bond-offs required to clear the bonder after an unsuccessful bond attempt need not be visible, shall not be cause for reject, and shall not be counted as a rebond.

A.3.4.3 Substrate wire rebonding or repair. Wire rebonding on substrates shall be permitted with the following limitations:

a. Scratched, open, or discontinuous substrate metallization paths or conductor pattern on a substrate, not caused by poor adhesion, may be repaired by bridging with or by the addition of bonded conductors having current carrying capacity at least 3.5 times the maximum calculated operating load current for the conductor or 3.5 times the current capacity of the wire bond connection terminating on the damaged conductor path. The quantity of repairs shall be limited to one for each one-half square inch or fraction thereof of substrate area.

b. No rebonds shall be made over intended bonding areas in which the top layer metallization has lifted, peeled, or has been damaged such that underlying metallization or substrate is exposed at the immediate bond site.

A.3.4.4 Compound bonding. Compound bonding for rework or repair is permitted only as follows:

a. A compound bond may be performed one time at a given location.

b. Only monometallic compound bonds are permitted (i.e., the original bond wire and that used for compound bonding shall be the same material).

c. The new bond shall cover at least 75 percent of the original bond or wire.

d. The maximum number of compound bonds shall not exceed 10 percent of the total number of wires.

e. A corrective action system shall be utilized in order to reduce the number of compound bonds.

f. All compound bonds shall be 100 percent nondestructive pull tested in accordance with MIL-STD-883, method 2023.

g. A compound bond shall not be used to connect two wires.

h. All compound bonds shall meet the visual criteria in MIL-STD-883, method 2017 and method 2032.

A.3.4.5 Element replacement. Element replacement shall be permitted with the following limitations:

a. Any polymer attached element may be replaced two times at a given location on any SSR.

b. Any metallic attached element may be replaced one time at a given location.

c. Any metallic attach element on a plated tab where the tab is attached to a substrate with a higher temperature metallic attach process, may be replaced two times.

d. Substrates may be removed and put into a new package one time.

A.3.4.6 Seal rework. It shall be permissible to perform seal rework without delidding on SSR's using hybrid technology that fail fine leak testing one time, only if tracer gas is included during the original sealing operation and under all of the following conditions:

a. Fine leak testing, without pressurization (bomb), shall be performed immediately after sealing prior to any other test.

b. SSR's shall be stored in a nitrogen environment for a maximum of 4 hours between initial seal and reseal without replacing the cover.

c. SSR's shall be submitted to a predetermined vacuum bake prior to reseal.

d. Only lid to package seals shall be resealed. Solder sealed packages may not be reworked in accordance with this procedure.

NOTE: The leak testing in A.3.4.6a shall not be used as a substitute for the fine leak testing required in MIL-STD-883.

A.3.4.7 Delidding of SSR's. Hybrid construction SSR's may be delidded and relidded for rework or repair provided the delid-relid procedures, controls, qualification plan, and resulting data are baselined and approved by the qualifying activity. The number of delid-relid cycles allowed shall be in accordance with A.3.4.7.1 or A.3.4.7.2. Delid-relid history (i.e., traceability by lot number or serial numbers) shall be maintained by the SSR manufacturer and shall be made available for qualifying activity review upon request.

A.3.4.7.1 Solder sealed SSR's. Solder sealed SSR's may be delidded-relidded one time.

A.3.4.7.2 Welded SSR's. Only seam sealed, overlapping pulse welded, or laser welded packages designed for delid-relid may be delidded-relidded. SSR's may be delidded-relidded two times. Delid-relid cycles in excess of two shall be performed only with the approval of the qualifying activity.

A.3.5. Internal conductors (class II (hybrid) technology only). Internal thin film conductors on a substrate (metallization stripes, contact areas, bonding interfaces, etc.) shall be designed so that in normal operation (at worst case specified operating conditions) a properly fabricated conductor shall not experience a current density in excess of the maximum allowable value shown below for the applicable conductor material:

Conductor material	Maximum allowable current density
Aluminum (99.99 percent pure or doped) without glassivation	2×10^5 A/cm²
Aluminum (99.99 percent pure or doped) glassivated	5×10^5 A/cm²
Gold	6×10^5 A/cm²
All other (unless otherwise specified)	2×10^5 A/cm²

The current density shall be calculated at the point of maximum current density (i.e., greatest current per unit cross section; see A.3.5.a) for the specified SSR and schematic or configuration.

a. Use a current value equal to the maximum continuous current (at full fanout for digitals or at maximum load for linears) or equal to the simple time-averaged current obtained at maximum rated frequency and duty cycle with maximum load, whichever results in the greater current value at the point of maximum current density. This current value shall be determined at the maximum recommended supply voltage and with the current assumed to be uniform over the entire conductor cross sectional area.

b. Use the minimum allowed metal thickness in accordance with manufacturing specifications and controls including appropriate allowance for thinning experienced in the metallization step (via). The thinning factor over a metallization step is not required unless the point of maximum current density is located at the step.

c. Use the minimum actual design conductor widths (not mask widths) including appropriate allowance for narrowing or undercutting experienced in metal etching.

d. Areas of barrier metals and nonconducting material shall not be included in the calculation of conductor cross section.

Thick film conductors on hybrid SSR's or multichip substrates (metallization strips, bonding interfaces, etc.) shall be designed so that a properly fabricated conductor shall not dissipate more than 4 watts/cm² when carrying maximum design current (except for conductors on BeO which shall dissipate no more than 82 watts/cm²).

A.3.6. SOLDER DIP (RETINNING) LEADS

A.3.6.1 Solder dip (retinning) leads (not applicable to terminal L). Only the manufacturer, at their option, may solder dip/retin the leads of product supplied to this specification provided the solder dip process (A.3.6.2) or equivalent processes has been approved by the qualifying activity.

A.3.6.2 Qualifying Activity Approval. Approval of the solder dip process will be based on one of the following options:

a. When the original lead finish qualified was hot solder dip in accordance with A.3.6.2b.(4). The manufacturer shall use the same solder dip process for retinning as is used in the original manufacture of the product.

b. When the lead originally qualified was not hot solder dip as prescribed in A.3.6.2a, approval for the process to be used for solder dip shall be based on the following test procedure:

(1) Six samples of any SSR of a individual specification sheet and specific lead finish shall be subjected to the manufacturer’s solder dip process. Following the test, the SSR's shall be subjected to the A2 and A3 tests of the group A inspection, solder dip process, the relays are subjected to the group A electricals. No process related (solder dip) defects are allowed.

(2) Two of the six samples shall then be subjected to the solderability test. No defects are allowed.

(3) The remaining four samples are subjected to the resistance to solder heat test and then to the A2 and A3 tests of the group A inspection. No process related (solder dip) defects are allowed.

(4) (4) In addition, the hot solder dip process shall meet requirements of 6.6.2.

A.3.6.3 Solder dip/retinning options. The manufacturer may solder dip/retin as follows:

a. After the group A, A1, screening tests. SSR's shall then be subjected to the remaining group A inspections.

b. As a corrective action, if the lot fails the group A solderability test:

c. After completion of group A inspection and following the solder dip/retinning process, an external visual examination in accordance with A3 of group A shall be repeated.

APPENDIX B

REQUIREMENTS FOR HYBRID MICROCIRCUIT ELEMENTS

B.1 SCOPE

B.1.1 Scope. This appendix establishes requirements for a component evaluation system for class II SSR's manufactured in accordance with this specification. The manufacturer shall maintain and demonstrate this system to the qualifying activity as prerequisite for qualification and retention of qualification. This appendix is a mandatory part of the specification. The information contained herein is intended for compliance.

B.2. APPLICABLE DOCUMENTS.

SPECIFICATIONS

DEPARTMENT OF DEFENSE

MIL-PRF-19500 - Semiconductor Devices, General Specification for.

MIL-PRF-38535 - Integrated Circuits (Microcircuits) Manufacturing, General Specification for.

STANDARDS

DEPARTMENT OF DEFENSE

MIL-STD-752 - Equipment Spectrum Signatures, Collection Standard for.

MIL-STD-790 - Standard Practice for Established Reliability and High Reliability Qualified Products List (QPL) Systems for Electrical, Electronic, and Fiber Optic Parts Specifications.

MIL-STD-883 - Test Methods and Procedures for Microelectronics.

B.3. REQUIREMENTS.

B.3.1 General requirements.

B.3.1.1 Relay class. The manufacturer shall establish a component evaluation system based on the class of the relay. There are two classes of relays defined in this specification: Class I which uses discrete device technology; and class II which uses hybrid technology. Class II requires the manufacturer to meet the requirements as specified herein.

B.3.1.2 Alternative system requirements. The manufacturer has the option to use alternative methods for achieving the general requirements of the component evaluation system specified herein. There are two methods for approving alternative system requirements:

a. Approval by the qualifying activity of proposals by the manufacturer.

b. When the qualifying activity has approved the establishment of a Technology Review Board (TRB) in accordance with MIL-STD-790, the TRB can approve alternative systems.

B.3.2 SSR element evaluation requirements. Herein, "SSR" refers to the hybrid or multichip microcircuit and hybrid/integrated circuits. Four phases of SSR element evaluation are required (see table B-I).

APPENDIX B

TABLE B-I. SSR element evaluation summary.

Requirements	Reference paragraph	Table
Microcircuit and semiconductor dice	B.3.3.2	B-II
Passive elements	B.3.3.3	B-III
Ceramic substrate printed wiring	B.3.3.4	B-IV
Process control	B.3.4	B-V

B.3.2.1 Sequence of testing. The preferred tests identified in tables B-II, B-III, and B-IV identify various subgroups of tests and within those subgroups a sequence of tests. The subgroups may be performed in any sequence, individual testing within a subgroup shall be performed in the sequence indicated. The manufacturer may use alternative systems provided they are approved as specified in B.3.1.2.

B.3.2.2 Protection from electrostatic discharge. For elements and SSR's that are sensitive to electrostatic discharge, handling precautions and grounding procedures shall be taken to protect the elements and SSR's from accidental damage.

B.3.3 Element evaluation.

B.3.3.1 General.

B.3.3.1.1 Element. Herein, "element" refers to materials for SSR assembly. Before SSR assembly, element characteristics shall be evaluated to assure their compatibility with SSR requirements and assembly procedures (see table B-I).

B.3.3.1.2 Characteristics. Characteristics to be verified shall be those necessary for compatibility with the element specification and assembly procedures, and at least those which cannot be verified after assembly but could cause functional failure of the SSR.

B.3.3.1.3 Location of element evaluation. Element evaluation may be performed at either the element supplier or SSR manufacturing facility.

B.3.3.2 Evaluation of microcircuit and semiconductor dice. Microcircuit and semiconductor die shall be evaluated as specified in B.3.3.2.1 through B.3.3.2.3. The manufacturer may use alternative evaluation systems provided they are approved as specified in the electrical test specifications.

B.3.3.2.1 Electrical test specifications. Electrical test parameter, values, limits (including deltas), and conditions shall be as specified in the microcircuit or semiconductor dice detail specification.

B.3.3.2.2 Die evaluation. Evaluation of the die shall include electrical and visual evaluation of the die as well as an evaluation of assembled die. The electrical and visual evaluation of the semiconductor are not required if the die is a JANCHC or JANCKC die tested in accordance with MIL-PRF-19500, appendix H. Electrical and visual evaluation of the microcircuit die is not required for MIL-PRF-38535 qualified die.

B.3.3.2.2.1 Electrical testing. Each die shall be electrically tested (100 percent of the lot), which may be done at the wafer level provided all failures are identified and removed from the lot when the dice are separated from the wafer. The requirements shall be specified by the manufacturer for compliance with the die specifications.

B.3.3.2.2.2 Visual inspection. Each die shall be visually inspected to assure conformance with the applicable die related requirements of MIL-STD-883, method 2012; MIL-STD-752, method 2072 and method 2073; and the die specification.

B.3.3.2.3 Assembled die evaluation. From each wafer lot, a sample shall be evaluated in accordance with table B-II and B.3.3.2.3.1 through B.3.3.2.3.2. Each sample shall be assembled into suitable packages that simulate the assembly methods and functional conditions of the element within the intended application.

B.3.3.2.3.1 Subgroup 1 and subgroup 2.

B.3.3.2.3.1.1 Sample size. The sample size shall be at least 10 dice from each wafer lot.

B.3.3.2.3.1.2 Subgroup 1 (internal visual). Each sample shall be visually inspected after assembly for conformance with the applicable die related requirements of MIL-STD-883, method 2012; MIL-STD-752, method 2072 and method 2073; and the element specification.

B.3.3.2.3.1.3 Subgroup 2 (electrical testing). Final electrical testing shall include static tests at 25°C, at maximum rated operating temperature, and at minimum rated operating temperature.

B.3.3.2.3.2 Subgroup 3.

B.3.3.2.3.2.1 Sample size. From each wafer lot, a sample of at least 5 dice requiring 10 bond wires minimum shall be selected.

B.3.3.2.3.2.2 Wire bond strength testing. For wire bond strength testing:

a. A minimum of ten wires, consisting of chip to package bonds, shall be destructively pull tested. An equal number of bonds shall be tested on each sample die.

b. For beam lead and flip-chips, five dice shall be tested.

c. The die metallization shall be acceptable if no failure occurs. If only one wire bond fails, another sample shall be selected in accordance with B.3.3.2.3.2.1 and subjected to subgroup 3 evaluation. If the second sample contains no failures, the bonding test results are acceptable. If the second sample contains one or more failures, or if more than one failure occurs in the first sample, the lot of dice shall be rejected.

d. The rejected wafer lot may be resubmitted to A3 evaluation if the failure was not due to defective die metallization.

TABLE B-II. Assembled dice evaluation requirements.

Subgroup	Test	MIL-STD-883		Quantity (accept no.)	Reference paragraph
		Method	Condition		
1	Internal visual	2010 2072 1/ 2073 1/	As applicable	10 (0)	B.3.3.2.3.1.2
2	Electrical			10 (0)	B.3.3.2.3.1.3
3	Wire bond evaluation	2011	As applicable	10 (0) wires or 20 (1) wires	B.3.3.2.3.2.2

1/ MIL-STD-750 methods.

B.3.3.3 Passive elements.

B.3.3.3.1 Electrical test specifications. Electrical test parameters, values, limits, and conditions shall be as specified in the passive element specification.

B.3.3.3.2 Evaluation of passive element lots. Evaluation of passive elements shall include electrical and visual evaluation of the elements as well as an evaluation of assembled elements. The electrical and visual evaluation of the element is not required if the element is an established reliability QPL or other QPL type device. The manufacturer may use alternative evaluation systems provided they are approved as specified in B.3.1.2.

B.3.3.3.2.1 Electrical testing. Each passive element shall be 100 percent electrically tested at 25°C, or as specified in the passive element specification.

B.3.3.3.2.2 Visual inspection. Each passive element shall be 100 percent visually inspected to assure conformance with the applicable passive element specification and the related requirements of MIL-STD-883, method 2032.

B.3.3.3.3 Assembled passive elements. From each inspection lot of passive elements, a randomly selected sample shall be evaluated in accordance with table B-III and B.3.3.3.3.1 through B.3.3.3.3.3.

a. Each sample shall be assembled into suitable packages that simulate the assembly methods and functional conditions of the element within the intended application.

b. The sample shall contain at least 20 wire bonds (an equal number on each element) if the wire bonding assembly is applicable.

B.3.3.3.3.1 Visual inspection (subgroup 1). Passive elements shall be visually inspected, using a sample of 22, to assure conformance with the applicable passive element specification and MIL-STD-883, method 2032.

B.3.3.3.3.2 Electrical testing of passive elements (subgroup 2). Passive elements shall be electrically tested, using a sample of 10, at 25°C ± 5°C for the following characteristics (minimum):

a. Resistors: dc resistance.

b. Ceramic type capacitors: DWV, insulation resistance, capacitance, and dissipation factor.

c. Tantalum type capacitors: dc leakage current, capacitance, and dissipation factor.

d. Inductors: dc resistance, inductance, and Q.

B.3.3.3.3.3 Wire bond strength testing (subgroup 3). The wire bond test only applies to passive elements when wire bond assembly of passive elements is used to manufacture the SSR. The sample shall include at least 5 elements and 10 bond wires minimum.

a. At least 10 wires, consisting of element to substrate and package bonds shall be destructively pull tested. An equal number of bonds shall be tested on each sample element.

b. The element metallization shall be acceptable if no failure occurs. If only one wire bond fails, a second sample shall be selected from the remaining elements in the evaluation sample, and subjected to the test per B.3.3.3.3.3a. If the second sample contains no failures the bonding test results are acceptable. If the second sample contains one or more failures, or if more than one failure occurs in the first sample, the element lot shall be rejected.

c. The element inspection lot may be resubmitted to evaluation if the failure was not due to defective element metallization.

TABLE B-III. Assembled passive element evaluation requirements.

Subgroup	Test	MIL-STD-883		Quantity (accept no.)	Reference paragraph
		Method	Condition		
1	Internal visual	2032	As applicable	22 (0)	B.3.3.3.3.1
2	Electrical			10 (1)	B.3.3.3.3.2
3	Wire bond evaluation	2011	As applicable	10 (0) wires or 20 (1) wires	B.3.3.3.3.3

B.3.3.4 Ceramic substrate printed wiring (substrates).

B.3.3.4.1 Definition. For the purpose of substrate evaluation, a substrate inspection lot shall consist of homogeneous substrates having the same number of layers, manufactured using the same facilities, processes, materials, and vacuum deposited, plated or printed as one lot.

B.3.3.4.2 Electrical test specifications. Electrical test parameters, values, limits, and conditions shall be as specified in the applicable substrate specification.

B.3.3.4.3 Evaluation of substrate element lots.

B.3.3.4.3.1 Electrical testing. Each substrate shall be electrically tested at 25°C, as specified in the applicable substrate detail specification.

B.3.3.4.3.2 Visual inspection. Each substrate shall be visually inspected to assure conformance with the applicable requirements of MIL-STD-883, method 2032, and the applicable substrate specification.

B.3.3.4.4 Evaluation of assembled substrate elements. From each inspection lot of substrates, a randomly selected sample shall be evaluated in accordance with table B-IV and B.3.3.4.4.1 through B.3.3.4.4.3. With preparing activity approval, destructive tests may be performed on test coupons which provide the required test data. The test coupons shall be made with the same materials that were used in the manufacturing of the inspection lot and processed at the same time as the inspection lot.

B.3.3.4.4.1 Subgroup 1. A minimum of five samples shall be submitted to subgroup 1 testing.

B.3.3.4.4.1.1 Physical dimension. Inspect in accordance with MIL-STD-883, method 2016, and the applicable substrate detail specification.

B.3.3.4.4.1.2 Visual inspection. Inspect in accordance with MIL-STD-883, method 2032, and the applicable substrate detail specification.

TABLE B-IV. Assembled substrate evaluation requirements

Subgroup	Test	MIL-STD-883		Quantity (accept no.)	Reference paragraph
		Method	Condition		
1	Physical dimension Visual inspection Electrical	2016 2032	As applicable As applicable	5 (0)	B.3.3.4.4.1.1 B.3.3.4.4.1.2 B.3.3.4.4.1.3
2	Conductor thickness or conductor resistivity Film adhesion Solderability			3 (1)	B.3.3.4.4.2.1 B.3.3.4.4.2.2 B.3.3.4.4.2.3 B.3.3.4.4.2.4
3	Temperature coefficient of resistance Wire bond evaluation Die sheer evaluation	 2011 2019	 	2 (0) 10 (0) wires or 20 (1) wires 2 (0)	B.3.3.4.4.3.1 B.3.3.4.4.3.2 B.3.3.4.4.3.3

B.3.3.4.4.1.3 Electrical. Substrates shall be electrically tested at 25°C for the following characteristics (minimum). Requirements shall be as specified in the applicable substrate detail specification.

a. Resistors: dc resistance.

b. Capacitors: Capacitance. If specified in the applicable substrate detail specification, test for DWV, insulation resistance, and dissipation factor.

c. For multilayered substrates, continuity and isolation testing shall be performed to verify the interconnection of conductors as specified in the applicable substrate detail specification.

B.3.3.4.4.2 Subgroup 2. A minimum of three samples that have been subjected to, and passed, subgroup 1 testing shall be submitted to subgroup 2 testing.

B.3.3.4.4.2.1 Conductor thickness. Measure conductor thickness in accordance with the applicable substrate detail specification. Conductor thickness shall meet the requirements specified in the applicable substrate detail specification.

B.3.3.4.4.2.2 Conductor resistivity. Measure conductor resistivity in accordance with the applicable substrate detail specification. Conductor resistivity shall meet the requirements specified in the applicable substrate detail specification.

B.3.3.4.4.2.3 Film adhesion. The manufacturer is responsible for establishing the appropriate test method for compliance with film adhesion specifications herein. The substrate and tape shall show no evidence of peeling or flaking of metallization.

B.3.3.4.4.2.4 Solderability. For solderable substrates only, perform solderability testing, if specified in the applicable substrate detail specification, in accordance with the applicable substrate detail specification.

B.3.3.4.4.3 Subgroup 3. A minimum of two samples that have been subjected to, and passed, subgroup 1 testing shall be submitted to subgroup 3 testing.

B.3.3.4.4.3.1 Temperature coefficient of resistance (TCR): When specified in the applicable detail specification, perform TCR testing for resistors in accordance with MIL-STD-202, method 324. TCR shall meet the requirements specified in the applicable substrate detail specification.

a. Thick film type: Test as a minimum, two resistors from each resistor paste sheet resistance value. One from the smallest and one from the largest area resistors at -55°C and +125°C using a reference reading at +25°C, or temperatures as specified in the substrate detail specification.

b. Thin film type: Test as a minimum, the highest value resistor at +125°C using a reference reading at +25°C or temperatures as specified in the substrate detail specification.

c. If specified in the applicable detail specification, TCR tracking testing shall be performed. TCR tracking shall meet the requirements specified in the applicable substrate detail specification.

B.3.3.4.4.3.2 Wire bond strength testing. For wire bondable substrates, perform wire bond strength testing in accordance with MIL-STD-883, method 2011. The sample shall include at least 2 substrates and 10 bond wires minimum.

a. At least 10 wires, consisting of substrate to substrate bonds, shall be destructively pull tested. An equal number of bonds shall be tested on each sample substrate.

b. The substrate metallization shall be acceptable if no failure occurs. If only one wire bond fails, a second sample of a minimum of 20 wires shall be prepared using the same wire type/size and the same type equipment as the failed bond. If the second sample contains one or more failures, or if more than one failure occurs in the first sample, then the substrate inspection lot shall be rejected.

c. The substrate inspection lot may be resubmitted to evaluation if the failure(s) was not due to defective substrate metallization.

B.3.3.4.4.3.3 Die shear strength testing. Perform shear strength testing in accordance with MIL-STD-883, method 2019. At least two dice per substrate shall be attached and tested for each die attachment method, as specified in the applicable substrate detail specification. If a failure occurs at less than the specified force and is not due to defective substrate materials, the lot shall be resubmitted to die shear evaluation and the failure mode documented.

B.3.4 Control of critical process and procedure (process control). The indicated process shall be controlled in accordance with table B-V and B.3.4.1.

TABLE B-V. Process control summary.

Operation	MIL-STD-883		Paragraph
	Method	Condition	
Wire bonding	2011 2023	As applicable	B.3.4.1

B.3.4.1 Wire bonding.

B.3.4.1.1 General. A process machine/operator evaluation shall be performed:

a. When a machine is put into operation.

b. Periodically while in operation, not to exceed 4 hours.

c. When the operator is changed.

d. When any machine part or an adjustment has been made.

e. When the spool of wire is changed or a new SSR production lot is started.

B.3.4.1.2 Test samples. Test samples that simulate the production SSR may be destructively evaluated in lieu of the product.

B.3.4.1.3 Process machines. Process machines not meeting the evaluation requirements shall not be used.

B.3.4.1.4 Corrective action of process machine. A process machine may be returned to operation only after appropriate corrective action has been implemented and the machine has been evaluated and passed testing in accordance with table B-V as required.

B.3.4.1.5 Data record. A data record shall be maintained and identifiable to each machine, operator, shift, and date of test.

B.3.4.1.6 Wire bonding. Wire bond strength testing shall be performed as follows:

B.3.4.1.6.1 Process machine/operator evaluation. A minimum sample of 10 wires total from 3 SSR's shall be destructively pull tested in accordance with MIL-STD-883, method 2011.

a. The sample shall consist of bonds to elements typical of SSR assembly operation.

b. Evaluation results are acceptable if no failure occurs below the present value given in table B-I of MIL-STD-883, method 2011. If any of the sample wires fail, the bonder shall be deactivated and corrective action taken. When a new sample has been prepared, tested, and passed this procedure, and the machine/operator has been certified or recertified, the sample can be returned to production.

B.3.4.1.7 Lot sample bond strength. From each wire bonding lot, a sample of at least two SSR's shall be nondestructively tested in accordance with MIL-STD-883, method 2023. SSR's with known visual wire bonding rejects shall not be excluded from this sample.

a. A wire bonding lot consist of SSR's that are consecutively bonded using the same set-up and wire, by one machine/operator during the same period not to exceed 4 hours.

b. In each sample SSR, at least 15 wires shall be tested including one wire from each type of transistor, diode, capacitor, and resistor chips, three wires from each type of integrated circuit, and five wires connecting package leads, as applicable. If there are less than 15 wires in the SSR, all wires shall be tested. Sample SSR's shall be inspected for lifted wires. Lifted wires shall be counted as nondestructive pull test failures.

c. The wire bonding lot shall be acceptable if no failure occurs. If one wire/bond fails another sample of two SSR's shall be selected and one hundred percent nondestructively tested. If the second sample contains no failures the wire bonding lot is acceptable. If the second sample also contains failure(s), or more than one wire/bond fails in the first sample, the bonding machine/operator shall be removed from operation.

d. The failures shall be investigated and appropriate corrective action shall be implemented. The machine/operator shall be recertified in accordance with B.3.4.1.6.1 before being returned to operation. All SSR's bonded since the previous certification (lot sample bond strength test) shall be subjected to one hundred percent nondestructive bond strength testing.

Custodians:
Army - CR
Navy - EC
Air Force - 85

Review activities:
Army - MI
Navy - OS
Air Force - 17, 99
NASA - NA

Preparing activity:
DLA - CC

(Project 5945-0980)

STANDARDIZATION DOCUMENT IMPROVEMENT PROPOSAL

INSTRUCTIONS

1. The preparing activity must complete blocks 1, 2, 3, and 8. In block 1, both the document number and revision letter should be given.

2. The submitter of this form must complete blocks 4, 5, 6, and 7.

3. The preparing activity must provide a reply within 30 days from receipt of the form.

NOTE: This form may not be used to request copies of documents, nor to request waivers, or clarification of requirements on current contracts. Comments submitted on this form do not constitute or imply authorization to waive any portion of the referenced document(s) or to amend contractual requirements.

I RECOMMEND A CHANGE:	**1. DOCUMENT NUMBER**	**2. DOCUMENT DATE (YYMMDD)**

3. DOCUMENT TITLE

4. NATURE OF CHANGE (Identify paragraph number and include proposed rewrite, if possible. Attach extra sheets as needed.)

5. REASON FOR RECOMMENDATION

6. SUBMITTER

a. NAME (Last, First, Middle initial)	b. ORGANIZATION	
c. ADDRESS (Include Zip Code)	d. TELEPHONE (Incl Area Code) (1) Commercial (2) AUTOVON (If applicable)	7. DATE SUBMITTED (YYMMDD)

8. PREPARING ACTIVITY

a. NAME Defense Supply Center Columbus (DSCC-VAM)	b. TELEPHONE (Include Area Code) (1) Commercial (614) 692-0542 (2) AUTOVON 850-0542
c. ADDRESS (Include Zip Code) 3990 East Broad Street Columbus, OH 43213-1199	**IF YOU DO NOT RECEIVE A REPLY WITHIN 45 DAYS, CONTACT:** Defense Quality and Standardization Office 5803 Leesburg Pike, Suite 1403, Falls Church, VA 22041-3466 Telephone (703) 756-2340 AUTOVON 289-2340